Announcement

The lecture on Electronic Circuits
will be read by prof. Bogdan Pankiewicz
at a room NE232, on 14th. Dec. 2017, from 9:15 to 11:00 AM.

For laboratory classes on Electronic Circuits:

1. get prepared - before coming to the class download please and study materials available at *www.ue.eti.pg.gda.pl/~bpa/ec*
2. class for group A of 10 students - room EA322, on 14th. Dec. 2017, from 14:15 to 17:00 PM;
3. class for group B of 10 students - room EA322, on 15th. Dec. 2017, from 14:15 to 17:00 PM.

Electronics – preparatory course

Semiconductor Devices

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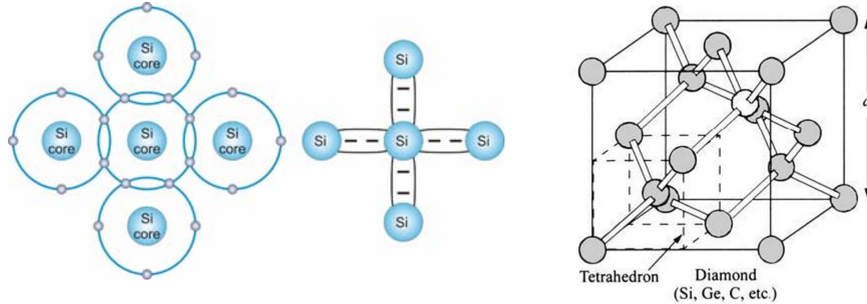
literature:

1. Ch.C. Hu, Modern Semiconductor Devices for Integrated Circuits, Prentice Hall 2009
   https://people.eecs.berkeley.edu/~hu/Book-Chapters-and-Lecture-Slides-download.html
2. A.S. Sedra, K.C. Smith, "Microelectronic Circuits", Oxford, 2007
3. Ch. Papadopoulos, "Solid-State Electronic Devices: An Introduction", Springer 2014
4. M. Grundmann, The Physics of Semiconductors: An Introduction Including Nanophysics and Applications, 2ed., Springer 2006
5. B. El-Kareh, L.N. Hutter, Silicon Analog Components: Device Design, Process Integration, Characterization, and Reliability, Springer 2015
6. S.M. Sze, Kwok K. Ng, "Physics of Semiconductor Devices", 3 ed., Wiley, 3 ed., 2006

Holes and electrons in semiconductors

Covalent bonding in Si crystal

5



An atom of Si crystal lattice shares its 4 valence electrons with 4 neighbour atoms, creating covalent bonds.

Schrödinger equation for a single electron in a crystal lattice

6

a – size of a crystal primitive cell.

Schrödinger equation for a single electron in a crystal lattice after many simplifications:

$$\left[-\frac{\hbar^2}{2m}\nabla^2 + V(\boldsymbol{r})\right]\Psi(\boldsymbol{r},\boldsymbol{k}) = E(\boldsymbol{k})\Psi(\boldsymbol{r},\boldsymbol{k})$$

gdzie

$$\hbar = \frac{h}{2\pi}$$

h – Planck constant;

$\boldsymbol{r} = (x,y,z)^T$ - vector of position in the XYZ space;

$\boldsymbol{k}$ - wave vector;

m – electron mass;

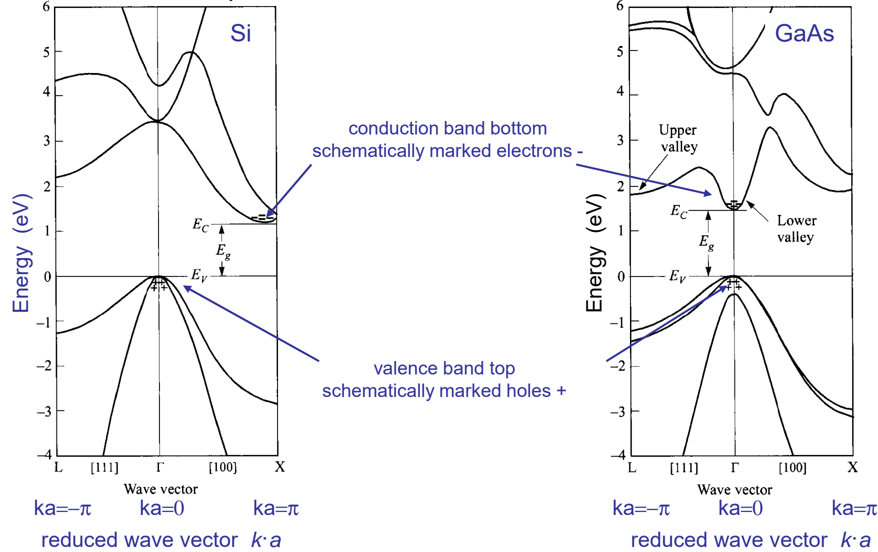
$V(\boldsymbol{r})$ – periodic potential energy function of electric field related to the periodic crystal lattice;

$E(\boldsymbol{k})$ – allowed values of electron energy (Eigenvalues);

$\Psi(\boldsymbol{r},\boldsymbol{k})$ – wave-function of the electron.

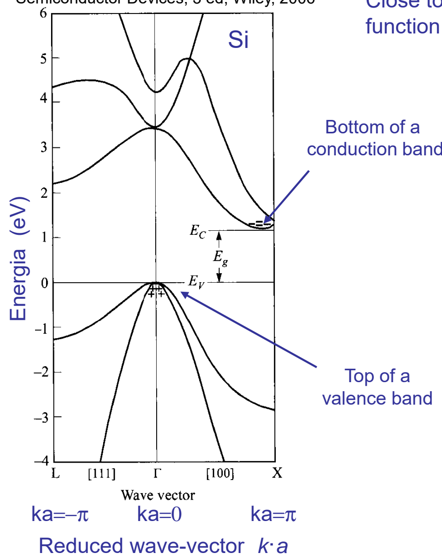
$E(\boldsymbol{k})$ dispersion - dependence of electron energy on wave vector $E(\boldsymbol{k})$ 7

S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006



Effective mass, group velocity and quasi-momentum of electron 8

S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006



Close to the local maxima and minima, the $E(\boldsymbol{k})$ function may be approximated with a parabolic expression

$$E(k) = E_0 + \frac{\hbar^2 k^2}{2m^*}$$

where m^* is the effective mass of electron

$$\frac{1}{m^*} = \frac{1}{\hbar^2}\frac{\partial^2 E(k)}{\partial k^2}$$

In ageneral case the effective mass is a tensor of m_{ij}^*

$$\frac{1}{m_{ij}^*} \equiv \frac{1}{\hbar^2}\frac{\partial^2 E(\boldsymbol{k})}{\partial k_i \partial k_j}$$

Group velocity of electron is expressed as

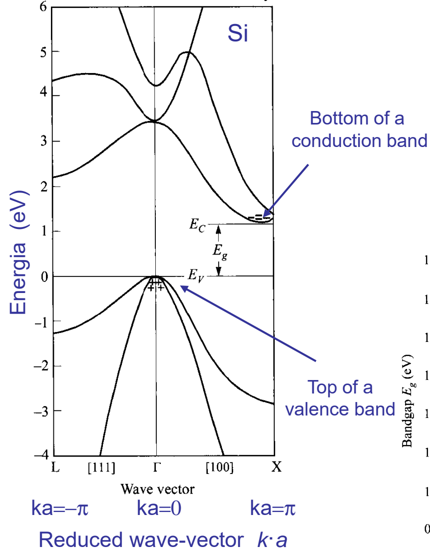
$$v_g = \frac{1}{\hbar}\frac{dE}{dk}$$

Quasi-momentum of electron is expressed as

$$p = \hbar k$$

Bandgap E_g – forbiden band

S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006



ka=–π ka=0 ka=π

Reduced wave-vector $k \cdot a$

Bottom of a conduction band

Top of a valence band

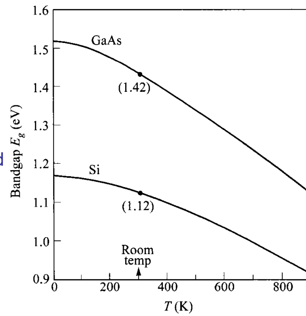
Neither electrons, nor holes can populate states in the bandgap (forbiden band)

$$E_v < E < E_c$$

where

$$E_g = E_c - E_v$$

bandgap value.



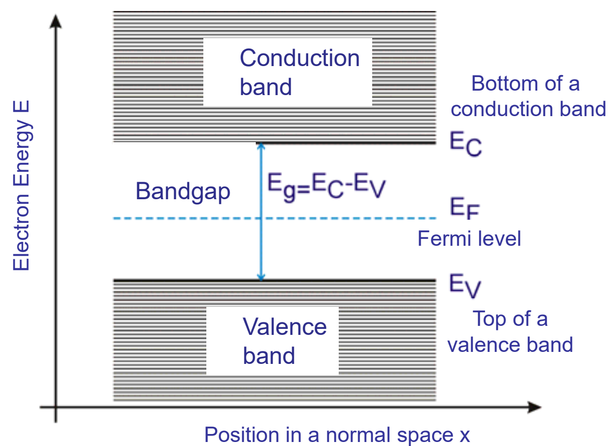
$E_g(T)$ dependence for Si and GaAs

	$E_g(0)$ (eV)	α (eV/K)	β (K)
GaAs	1.519	5.4×10^{-4}	204
Si	1.169	4.9×10^{-4}	655

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta}$$

Band structure of electron energy in a crystal

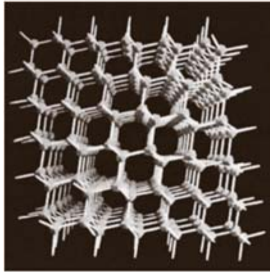
- Pauli exclusion principle requires splitting of electron energy levels of separated atoms into energy bands in a crystal.
- Electrons present in the conduction band, can move (nearly) freely there.



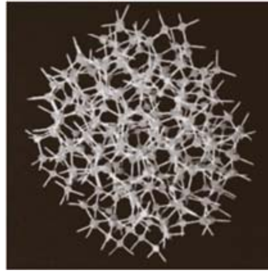
- Holes – missing electrons – present in the valence band can move (nearly) freely there.
- Electrons of the valence band and lower bands can not move freely.

Strukt_pasmowa_2

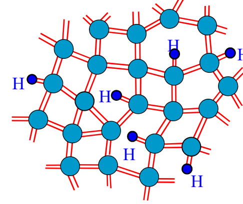
Energetic structure of amorphous semiconductors



Schematic picture of periodic bonds of Si atoms in a monocrystal



Schematic picture of amorphous Si. Its structure has many defects - missing atoms, „dangling" bonds.... There is no far distance order.



Two-dimensional schematic picture of amorphous Si with „dangling" bonds terminated with hydrogen atoms. Note: - number of hydrogen atoms is lower in real crystal.

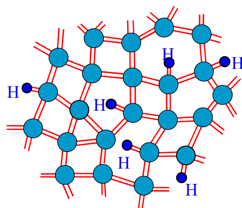
Amorphous semiconductor:

- No periodic order of far distance.
- Periodic order of short distance - typically at a distance of 1 nm.
- Large defect concentration.

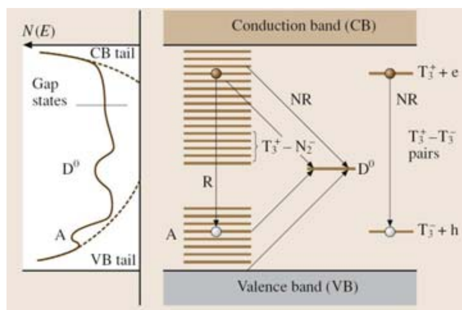
Kasap, Capper, Springer Handbook of Electronic and Photonic Materials, 2006

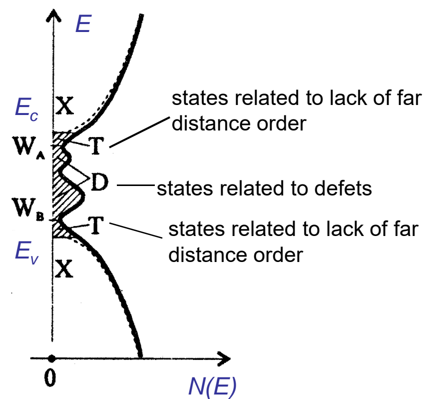
S.O.Kasap, Principles of Electronic Materials and Devices, McGraw-Hill, 2002

Energetic structure of amorphous semiconductors



Two-dimensional schematic picture of amorphous Si with „dangling" bonds terminated with hydrogen atoms. Note: - number of hydrogen atoms is lower in real crystal.



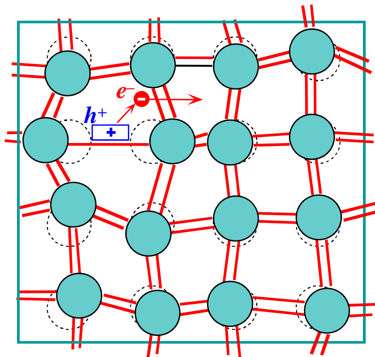


Dependence of state density on energy $N(E)$

Density of states in the energy interval of $E_v < E < E_c$ is not equal to 0, in contrast to a monocrystal.

M.Polowczyk, E.Klugmann, Przyrządy Półprzewodnikowe", Wyd.PG, 2001

Intrinsic semiconductor - monocrystal



Thermal vibrations of atoms can break bonds and thereby create electron-hole pairs.

S.O.Kasap, Principles of Electronic Materials and Devices, McGraw-Hill, 2002

There should be no electrons in the conduction band and no holes in the valence band in an ideal crystal at the absolute zero temperature.

At $T > 0$ K thermal vibrations of atoms result in breaking of some bonds. This is generation of electron-hole pairs. Their intrinsic concentrations are equal $n_i = p_i$.

Electrons in the conduction band and holes in the valence band are called charge carriers – they contribute to electric current.

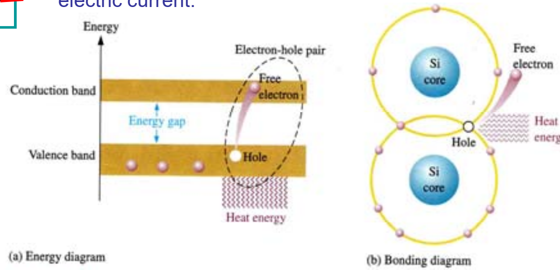
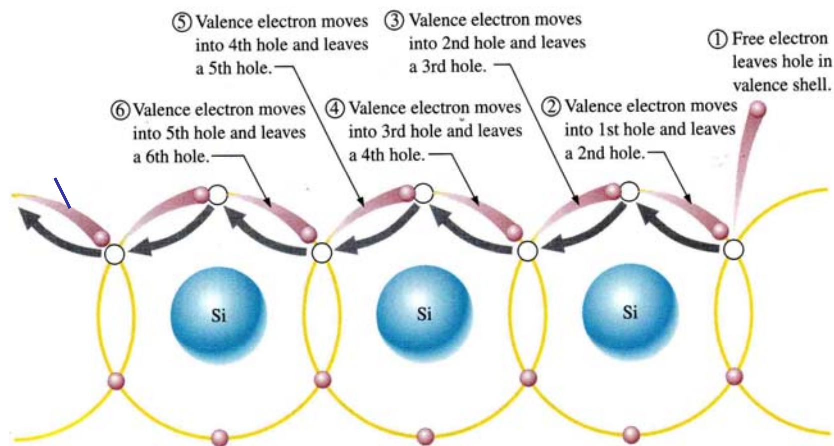


FIGURE 1–11
Creation of an electron-hole pair in an excited silicon atom. An electron in the conduction band is a free electron.

T.Floyd, Electronic Devices, Prentice-Hall, 1999

Free hole motion in the valence band

T.Floyd, Electronic Devices, Prentice-Hall, 1999



Doped semiconductors

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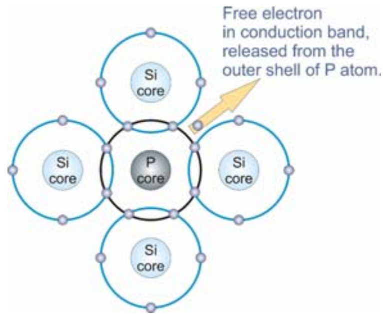
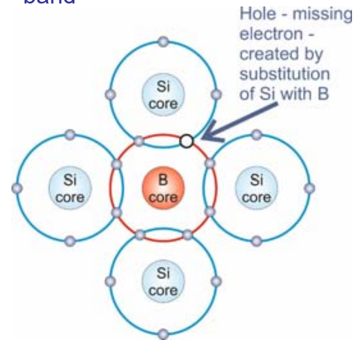
n – type semiconductors, intentionally doped to have large concentration of electrons in conduction band



P, As, Sb –donor dopants at Si

Donor concentration is denoted as N_D

p – type semiconductors, intentionally doped to have large concentration of holes in valence band



B, Ga, In –acceptor dopants at Si

Acceptor concentration is denoted as N_A

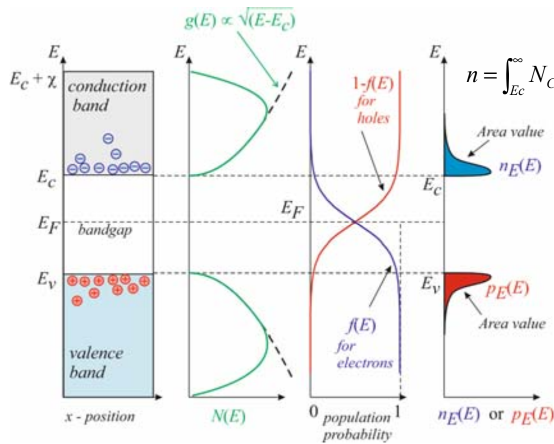
T.Floyd, Electronic Devices, Prentice-Hall, 1999

koncentracja *n* -2

Electron and hole concentrations

16

Electron *n* and hole *p* concentrations depend on density of energetic states *N(E)* and on probability of their population by electrons *f(E)*.



$$n = \int_{Ec}^{\infty} N_C(E) f(E) dE$$

Fermi-Dirac function – probability of population of electron states *f(E)*

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)}$$

E_F –Fermi energy; mean value of electron energy at the thermal equillibrium

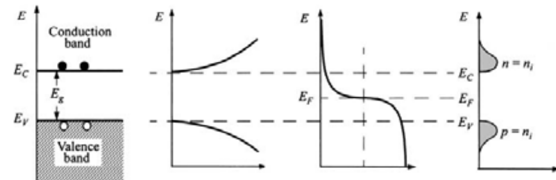
k_B - Boltzmann constant, k_B = $1{,}38 \cdot 10^{-23}$ J/K

$$p = \int_{-\infty}^{Ev} N_V(E)[1 - f(E)]dE$$

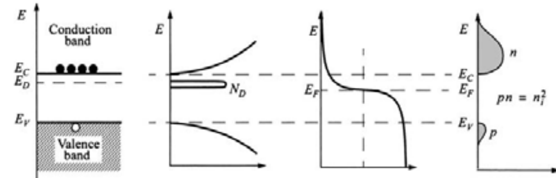
Poziom Fermiego E_F - 4

Fermi Level E_F

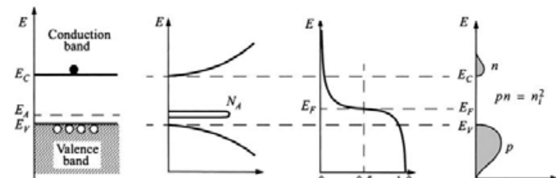
S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006



intrinsic semiconductor



n-type semiconductor
(of large electron concentration, doped with donors)



p-type semiconductor
(of large hole concentration, doped with acceptors)

$N(E)$ | $F(E)$ | n and p

Energy bands

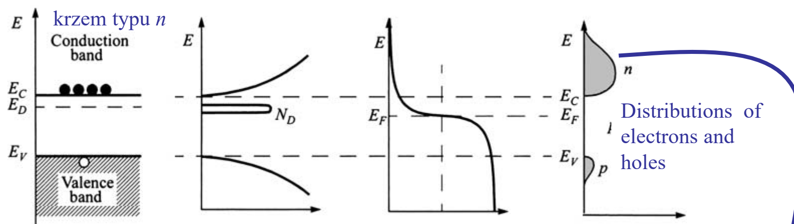
Densities of states

Probability functions for electrons

Population of bands with electrons and holes

Ruch termiczny nośników -1

Thermal motion of electrons and holes in semiconductor



electron energy
$$E = E_c + \frac{m_n^* v^2}{2}$$
potential | kinetic

Average energy of a thermal motion for an electron

$$E_{mnth} = \frac{m_n^* v_{mnth}^2}{2}$$

$$E_{mnth} = \frac{3}{2} k_B T$$

Average velocity of a thermal motion for an electron

$$v_{mnth} = \sqrt{\frac{3 k_B T}{m_n^*}}$$

(k_B –Boltzmann constant)

(Si, 300 K – v_{thav} = 200 km/s)

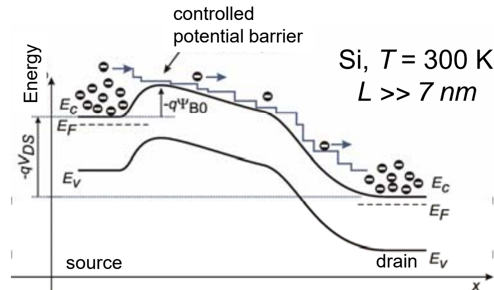
Mechanisms of electron and hole transport

Diffusion and drift in electric field

$L >> \lambda_{mn}$

L – length of electron path in a device.

For silicon, at $T = 300$ K λ_{mn} mean free path of electrons between collisions with crystal lattice is about 7 nm.



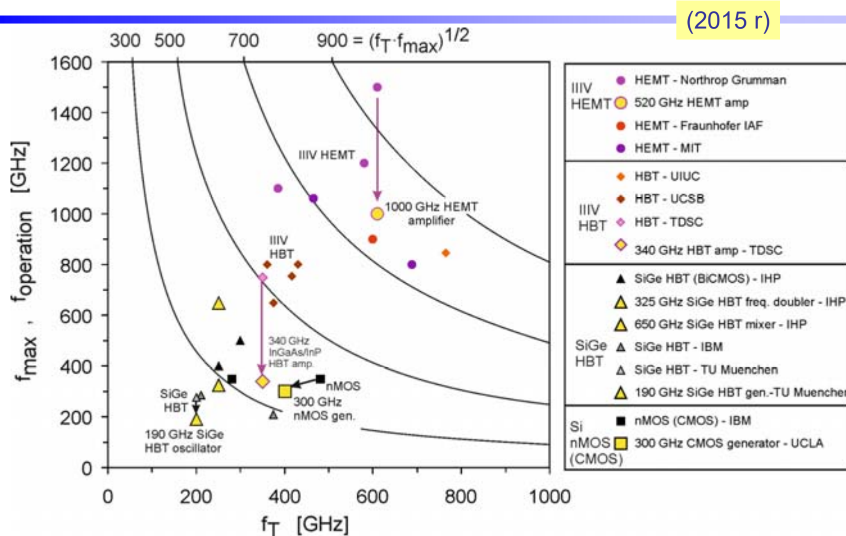
- For currently produced devices the lengths of electron paths are so long, that electrons many times collide with Si atoms. Their energies and momenta relax.
- It is convenient to use an average drift velocity of electrons in electric field $\mathscr{E}$ on their ways between scattering events.
- Carrier transport is described with ideas of:

  dyffusion,

  and drift in electric field $\mathscr{E}$ with velocity averaged for the thermal motion.

Record high f_T i f_{max} values for transistors and requencies of circuit operations $f_{circuit}$

(2015 r)



f_{max} – power-gain cut-off frequency a transistor - the highest frequency at which the the power-gain of the transistor is not smaller than 1

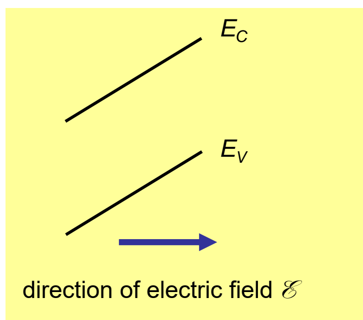
f_T – current-gain cut-off frequency a transistor - the highest frequency at which the the current-gain of the transistor is not smaller than 1

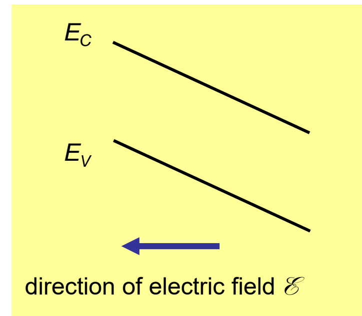
Semiconductor in electric field

E – energy
$\mathscr{E}$ – intensity of electric field
Ψ – electric potential
q – elementary charge, q = -e ≈ 1,6·10^{-19} C = 1,6·10^{-19} A·s

$$E = -q \cdot \Psi$$

$$\mathscr{E} = -\frac{d\Psi}{dx} = \frac{1}{q} \cdot \frac{dE}{dx}$$





pojecie ruchliwości

Mobility of electrical charge carriers in semiconductor

For long devices, when carrier scatering can not be neglected

$$L >> \lambda_{mn}$$

- Electrons (holes) are many times scattered.
- At the background of this chaotic thermal motion only the average drift velocities $\boldsymbol{v}_{drift}$ in external electric field $\mathscr{E}$ are considered.
- For low $\mathscr{E}$ the <u>average</u> drift velocity of electrons v_{driftn}:

$$\boldsymbol{v}_{driftn} = -\mu_n \mathscr{E}$$

- For low $\mathscr{E}$ the <u>average</u> drift velocity of holes v_{driftp}:

$$\boldsymbol{v}_{driftp} = \mu_p \mathscr{E}$$

ruchliwość - domieszkowanie

Mobility of electrical charge carriers in semiconductor

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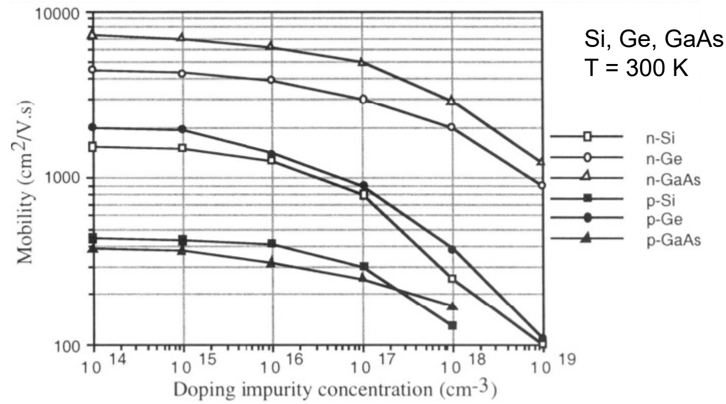
Mobility valueses of electrons and holes, μ_n oraz μ_p, for Si result from scattering at:

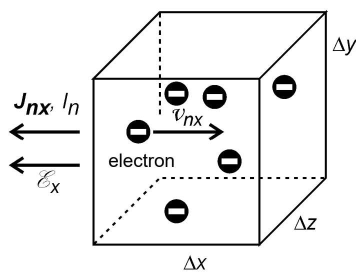
- thermal vibrations of crystal lattice
- dopant atoms –donors and acceptors.



J.-P. Colinge, C.A. Colinge, "Physics of Semiconductor Devices", Springer 2002

Drift current in electric field

24



Apply an electric field $\mathscr{E}_x$ to an Si sample. Electrons drift to the right with an average velocity of v_{nx}. During the time interval of

$$\Delta t = \Delta x / v_{nx}$$

all electrons from this $\Delta x \Delta y \Delta z$ cube escape through the right wall. The electron current may be expressed as:

$$\Delta I_n = -\frac{\Delta Q}{\Delta t} = -\frac{qn\Delta x \Delta y \Delta z}{\Delta t} = -qnv_x \Delta y \Delta z$$

Density of electron current J_{nx} is expressed as:

$$J_{driftnx} = \frac{\Delta I_n}{\Delta y \Delta z} = -qnv_{nx}$$

thus

$$J_{driftnx} = qn\mu_n \mathscr{E}_x$$

Drift current in electric field

For constant electrons n and holes p concentrations:

$$J_{driftnx} = qn\mu_n\mathscr{E}_x \qquad J_{driftpx} = qp\mu_p\mathscr{E}_x$$

$J_{driftnx}$ and $J_{driftpx}$ are electron and hole components of the drift current J_{driftx} in the direction of x.

$$J_{driftx} = qn\mu_n\mathscr{E}_x + qp\mu_p\mathscr{E}_x$$

Conductivity σ (characteristic conductance, inverse of characteristic resistance – reistivity ρ)

$$\sigma = \frac{1}{\rho} = \frac{J_{drifx}}{\mathscr{E}_x} = qn\mu_n + qp\mu_p$$

It happens often for an n-type semiconductor, that

$$n_n \approx N_D >> p_n \approx \frac{n_i^2}{n_n}$$

Drift current in electric field

It happens often for an n-type semiconductor, that

$$n_n \approx N_D >> p_n \approx \frac{n_i^2}{n_n}$$

thus

$$J_{driftnx} >> J_{driftpx}$$

$$J_{driftx} \approx J_{driftnx} = qn\mu_n\mathscr{E}_x$$

Conductivity σ (characteristic conductance, inverse of characteristic resistance – reistivity ρ)

$$\sigma = \frac{1}{\rho} \approx qn\mu_n$$

dziurowy prąd unoszenia

Drift current in electric field

It happens often for a p-type semiconductor, that

$$p_p \approx N_A >> n_p \approx \frac{n_i^2}{p_p}$$

thus

$$J_{driftpx} >> J_{driftnx}$$

$$J_{driftx} \approx J_{driftpx} = qp\mu_p \mathscr{E}_x$$

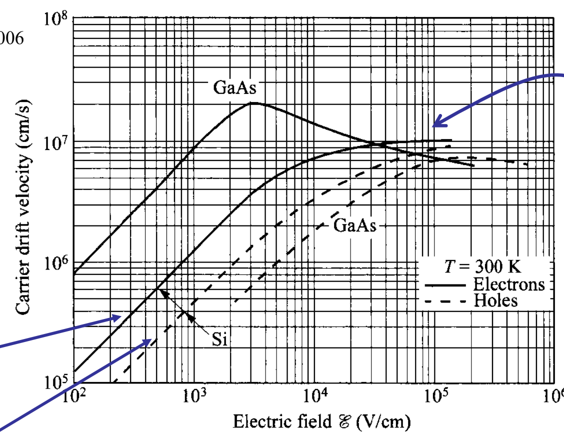
Conductivity σ (characteristic conductance, inverse of characteristic resistance – reistivity ρ)

$$\sigma = \frac{1}{\rho} \approx qp\mu_p$$

vdrift vs. E

Dependence of drift velocity on electric field intensity

S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006



For small intensities of electric field $\mathscr{E}$

$$v_{driftn} = -\mu_n \mathscr{E}$$

$$v_{driftp} = \mu_p \mathscr{E}$$

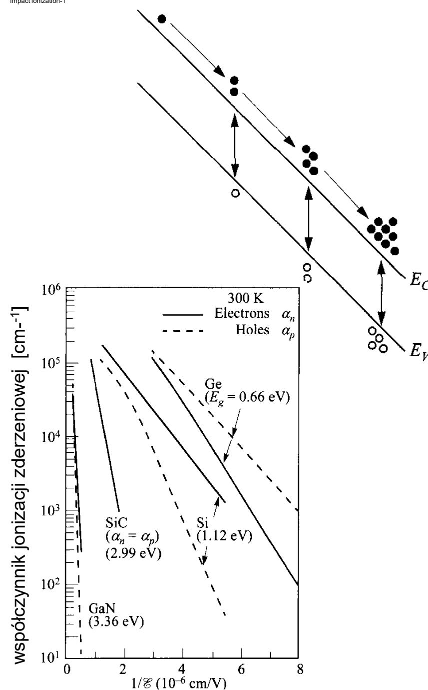
For large intensities of electric field $\mathscr{E}$, at silicon $\mathscr{E} > 10^4$ V/cm

$v_{driftn} = v_{satn}$

$v_{driftp} = v_{satp}$

impact ionization-1

Impact ionization – mechanism of avalanche breakdown



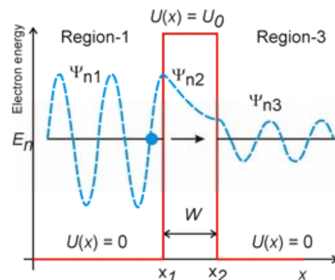
At very large intensities of elecctric field ℰ, 10^6 V/cm at Si, despite the scattering, some electrons or holes gain so high energies that an impact ionization is possible

- electron of a conduction band passes its excess energy to an electron of the valence band, and the energy is higher thaan the bandgap – there is created an additional electron-hole pair;
- this process may proceed in an avalanche manner – avalanche breakdown.

S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006

Electron_tunneling_2

Current of electrons tunneling through a rectangular barrier



S.M. Sze, K.K. Ng, "Physics of Semiconductor Devices", 3 ed., Wiley 2007, p. 48

A.F.J. Levi, "Applied Quantum Mechanics" 2ed., Cambridge Univ. Press, 2006, pp. 145-149 and 182-188

$T_t(E)$ – probability of tunneling of an electron having energy E_n:

$$T_t(E_n) = \left[1 + \left(\frac{k_1^2 + k_2^2}{2k_1k_2}\right)^2 \sinh^2(k_2W)\right]^{-1}$$

here: $k_1 = \sqrt{2m^* E_n}/\hbar$, $\quad k_2 = \sqrt{2m^*(U_0 - E_n)}/\hbar$

J_T – current density of tunneling electrons:

$$J_T = \frac{qm^*}{2\pi^2\hbar^3}\int_{Ec}^{\infty} f_1(E_n)\cdot N_{C1}(E_n)\cdot T_t(E_n)\cdot[1 - f_3(E_n)]\cdot N_{C3}(E_n)\,dE_n$$

N_{C1}, N_{C3} – densities of electron states in regions 1 and 3;
f_1, f_3 – Fermi-Dirac probability functions of population of electron states $f(E)$ in regions 1 and 3.

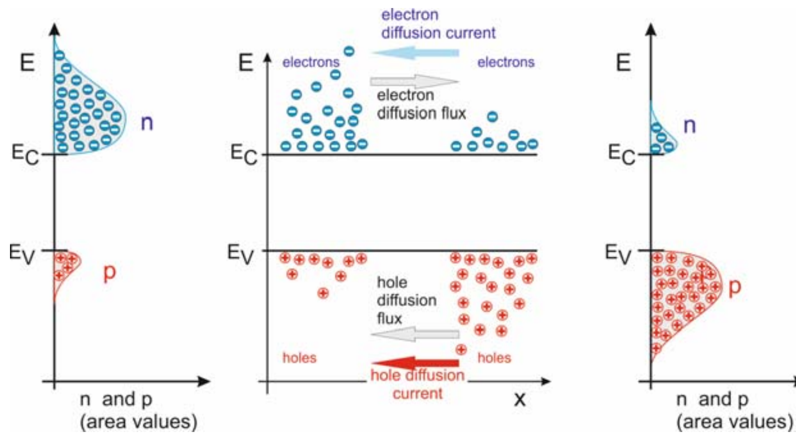
$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_BT}\right)}$$

Diffusion currents of electrons and holes

For long devices, when carrier scatering can not be neglected

$$L >> \lambda_{mn}$$

- Suppose that we have a not uniform distribution of electrons or holes.
- In this situation there are present fluxes of electron and hole diffusion, that is diffusion current – „trying to equillibrate the concentrations".
- Diffusion current may be nonzero even when the intensity of the electric field $\mathscr{E}$ is equal to zero.



Diffusion currents of electrons and holes

- Suppose that we have a not uniform distribution of electrons or holes.
- In this situation there are present fluxes of electron and hole diffusion, that is diffusion current – „trying to equillibrate the concentrations".
- Diffusion current may be nonzero even when the intensity of the electric field $\mathscr{E}$ is equal to zero.

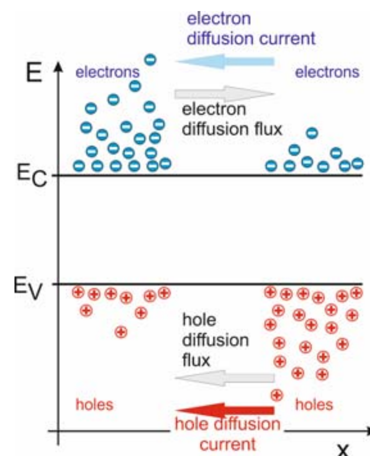
$$J_{difnx} = qD_n \frac{dn}{dx}$$

$$J_{difpx} = -qD_p \frac{dp}{dx}$$

where the diffusion costants D_n and D_p were determined by Einstein:

$$D_n = \mu_n \frac{k_B T}{q}$$

$$D_p = \mu_p \frac{k_B T}{q}$$



Density of conduction current *J* in semiconductor

Density of an electron component of conduction current J_n in a semiconductor is a sum of a component related to the drift in electric field $\mathscr{E}$ and of a component related to the diffusion:

$$J_{nx} = J_{driftnx} + J_{difnx}$$

$$J_{nx} = qn\mu_n \mathscr{E}_x + qD_n \frac{dn}{dx}$$

Density of a hole component of conduction current J_p

$$J_{px} = J_{driftpx} + J_{difpx}$$

$$J_{px} = qp\mu_p \mathscr{E}_x - qD_p \frac{dp}{dx}$$

Density of a conduction current J in a semiconductor :

$$J_x = J_{nx} + J_{px}$$

Diffusion constant value – *Einstein relation*

- Let us take a semiconductor sample, e.g Si, nonuniformly doped with donors.
- Let it be in thermodynamic equillibrium, which requires:

$$J_{nx} = 0 \qquad \text{or} \qquad 0 = qn\mu_n \mathscr{E}_x + qD_n \frac{dn}{dx}$$

We take into account that n and $\mathscr{E}_x$ may be expressed as:

$$n \approx N_C^* \exp\left(-\frac{E_c - E_F}{k_B T}\right) \qquad \mathscr{E}_x = \frac{1}{q}\frac{dE_c(x)}{dx}$$

Taking into account that $\frac{dE_F(x)}{dx} = 0$ in thermodynamic equillibrium,

we calculate: $\frac{dn}{dx} \approx -\frac{N_C^*}{k_B T} \exp\left(-\frac{E_c - E_F}{k_B T}\right) \cdot \frac{dE_c}{dx} = -\frac{n}{k_B T} \cdot \frac{dE_c(x)}{dx}$

The expression for J_{nx} takes form of: $0 = n\mu_n \frac{dE_c(x)}{dx} - nD_n \frac{q}{k_B T} \cdot \frac{dE_c(x)}{dx}$

We see that D_n may be expressed as: $D_n = \mu_n \frac{k_B T}{q}$

Similarly, D_p may be expressed as: $D_p = \mu_p \frac{k_B T}{q}$

Note: at room temperature $T \approx 300$ K thermal voltage V_T

$$V_T \equiv \frac{k_B T}{q} \approx 25 \text{ mV}$$

Electric field $\mathscr{E}$ in nonuniformly doped semiconductor

- Let us take a semiconductor sample, e.g Si, nonuniformly doped with donors or acceptors.
- Let it be in thermodynamic equillibrium, which means:

$$pn = n_i^2 \quad \text{and} \quad J_{nx} = 0$$

thus $$0 = qn\mu_n \mathscr{E}_x + qD_n \frac{dn}{dx}$$

We see that the drift current component and the diffusion current component compensate each other. We substitute the Einstein expression for the diffusion constant D_n:

$$D_n = \mu_n \frac{k_B T}{q}$$

The obtained electric field $\mathscr{E}_x$ at nonuniformly doped semiconductor is nonzero at equillibrium:

$$\mathscr{E}_x = -\frac{k_B T}{q} \cdot \frac{1}{n(x)} \frac{dn(x)}{dx} \qquad \mathscr{E}_x = \frac{k_B T}{q} \cdot \frac{1}{p(x)} \frac{dp(x)}{dx}$$

For n-type semiconductor, when $n \approx N_D >> n_i$:

$$\mathscr{E}_x = -\frac{k_B T}{q} \cdot \frac{1}{N_D(x)} \frac{dN_D(x)}{dx}$$

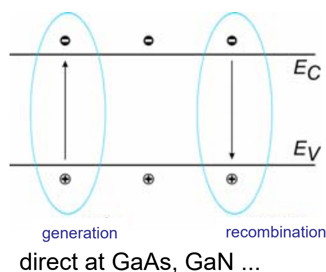
For p-type semiconductor, when $p \approx N_A >> n_i$:

$$\mathscr{E}_x = \frac{k_B T}{q} \cdot \frac{1}{N_A(x)} \frac{dN_A(x)}{dx}$$

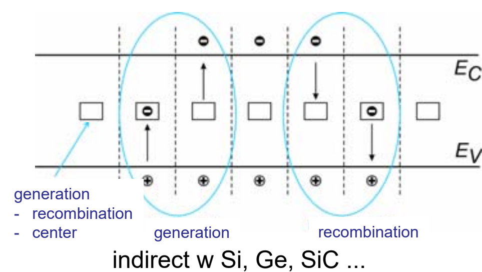
Generation and recombination of electrons and holes

- Generation and recombination processes take place in semiconductors;
- spontaneously – as an effect of thermal vibration of crystal lattice,
- or stimulated, eg. by illumination.

Generation and recombination models



direct at GaAs, GaN ...



indirect w Si, Ge, SiC ...

Let there be no current flow in the semiconductor sample.

$$\frac{\partial n}{\partial t} = G_n - U_n = G - \frac{n - n_0}{\tau} \qquad \frac{\partial p}{\partial t} = G_p - U_p = G - \frac{p - p_0}{\tau}$$

Generation caused by an external excitation.

Decay of the excess carriers - *return to equillibrium*

n_0, p_0 - equillibrium concentrations of electrons and holes.
G_n, G_p - electron and hole generation rates.
U_n, U_p - electron and hole recombinationrates.
G - Generation rate (or recombination rate – if negative) due to an external excitation.
$\tau_n = \tau_p = \tau$ - lifetime of excess electrons and holes.

An n-type Si sample was uniformly illuminated with light of quantum energy of radiation larger than E_g. The illumination was turned off at $t = 0$. How does the hole concentration p_n change in time?

$$\frac{\partial p}{\partial t} = G - \frac{p_n - p_{n0}}{\tau}$$

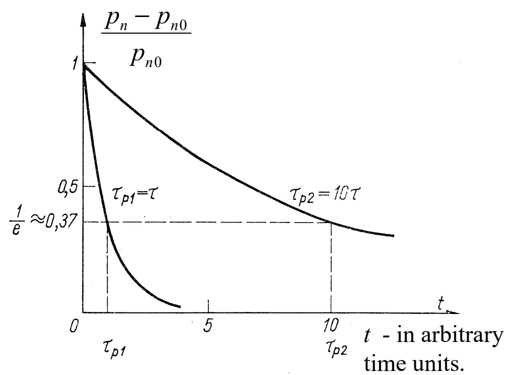
$p_{n0} \approx n_i^2/N_D$ - equillibrium concentration of holes.
$\tau_n = \tau_p = \tau$ - lifetime of excess electrons and holes.

$G(t<0) > 0$
$G(t\geq 0) = 0$

G – rate of generation caused by illumination.

Solutions for two different values of excess carrier lifetime.

$\tau = \tau_{p1}$ and $\tau = \tau_{p2} = 10\,\tau_{p1}$

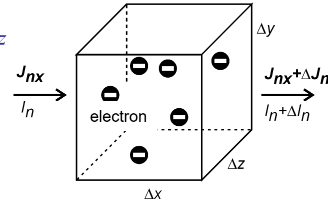


t - in arbitrary time units.

Equation of charge continuity

Let us neglect generation and recombination process.

An electron current of $I_{nx} = J_{nx}\,\Delta y\Delta z$ flows into a cube of $\Delta x\Delta y\Delta z$



while the current of $I_{nx} + \Delta I_{nx} = (J_{nx} + \Delta J_{nx})\Delta y\Delta z$ flows out.
The differece of ΔI_{nx} charges the element of $\Delta x\Delta y\Delta z$:

$$\Delta Q = -\Delta I_n \cdot \Delta t$$

$$\Delta Q = -q\partial n\Delta x\Delta y\Delta z \qquad -\Delta I_n \cdot \partial t = -\Delta J_n \cdot \Delta y\Delta z \cdot \partial t$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial \boldsymbol{J}_n}{\partial x}$$

After accounting for the generation G_n and recombination U_n we obtain the continuity equation for electrons:

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\frac{\partial \boldsymbol{J}_n}{\partial x}$$

Similarly - the continuity equation for holes:

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\frac{\partial \boldsymbol{J}_p}{\partial x}$$

Basic equations for analysis of semicoductor device operation

Poisson equation – for potential distribution Ψ:

$$\frac{\partial^2 \Psi}{\partial x^2} = \frac{q\left(n - p + N_A^- - N_D^+\right)}{\varepsilon\varepsilon_0}$$

Continuity equation for electrons:

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\frac{\partial \boldsymbol{J}_n}{\partial x}$$

Continuity equation for holes:

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\frac{\partial \boldsymbol{J}_p}{\partial x}$$

Density of electron conduction current:

$$J_{nx} = qn\mu_n\mathscr{E}_x + qD_n\frac{dn}{dx}$$

Density of hole conduction current:

$$J_{px} = qp\mu_p\mathscr{E}_x - qD_p\frac{dp}{dx}$$

Density of totalconduction current :

$$J_x = J_{nx} + J_{px}$$

NOTE:

They may be applied only for long devices, when carrier scatering can not be neglected.

$$L >> \lambda_{mn}$$

This equation set is used in computer simulation of devices. Apropriate boundary and initial conditions have to be applied also in these simulations. Analytical solutions require many simplifications.

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Introduction to operation and construction of Si MOSFETs

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Static characteristics of a metal oxide semiconductor field-effect transistor (MOSFET) with an enhanced channel

Most important assumptions (simplifications)

- Average drift velocity v_{driftn} of electrons is proportional to the electric field $\mathscr{E}$:

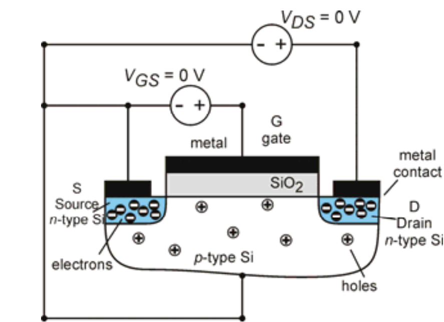
$$v_{driftn} = -\mu_n \mathscr{E}_x$$

- The current is conducted in extremely thin layer of the channel, having two-dimensional charge density of Q_{invn}.

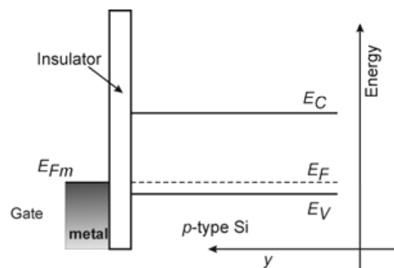
- Ohm law expressed in terms of electron concentration n and $\mathscr{E}$:

$$J_n = qn\mu_n \mathscr{E}_x \rightarrow I_D = -WQ_{invn}\mu_n \mathscr{E}_x$$

Zero V_{GS} and V_{DS} voltages



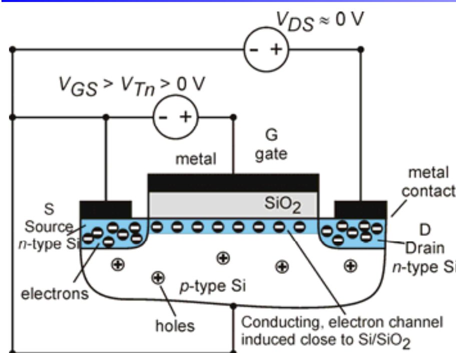
- Equilibrium electron concentration n in Si is extremely small, eg. 10^2 cm^{-3}.
- Equilibrium hole concentration p in Si is large, eg. 10^{18} cm^{-3}.
- Thus, there is no continuous electron conduction path between source and drain. Potential barrier, Ψ_B at the n source perimeter is high.
- Therefore, drain current I_D is negligible even when V_{DS}>0 V.



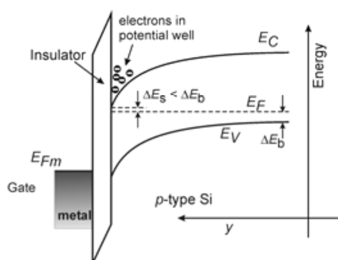
Idealized flat-band diagram

Equal work functions and no trapped charge assumed.

V_{GS} greater than threshold voltage V_{Tn} , $V_{DS} \approx 0$ V



- Si under SiO_2 interface in a state of strong inversion.
- Transistor „turned ON" $V_{GS} > V_{Tn} > 0$ V.
- Conducting channel of n-type created between source and drain.
- Applying $V_{GS} = V_{Tn} > 0$ results in lowering potential barrier Ψ_B to negligibly small value – for transistor with drift-diffusion transport.
- When $V_{DS} > 0$ V then a current I_D flows, carried by electrons.



Idealized band diagram

$V_{GS} > V_{Tn}$, 0 V < $V_{DS} < V_{GS} - V_{Tn}$

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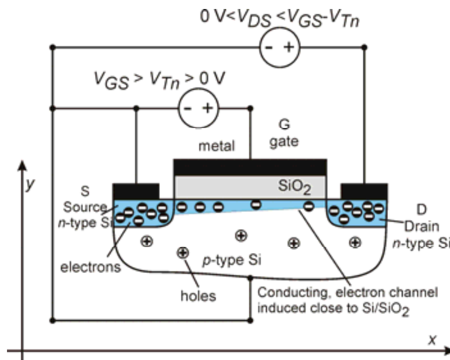

- Si under SiO_2 interface in a state of strong inversion.
- Drain current I_D. flows.
- Wzdłuż kanału o długości L przepływ Flow of I_D influences a potential distribution $\Psi(x)$ along the channel of L length:

$\Psi(x=0)$ = 0 V
$\Psi(x=L)$ = V_{DS}

where
x=0 at source edge,
x=L at drain edge.

- The voltage V_G(x) between the metal gate and the channel changes along the channel as:

$$V_G(x) = V_{GS} - \Psi(x)$$

Charge of electrons in a channel

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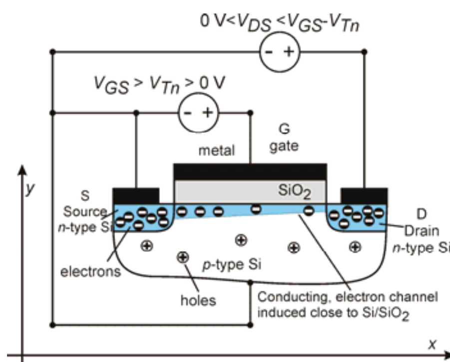
$V_{GS} > V_{Tn}$, 0 V < $V_{DS} < V_{GS} - V_{Tn}$



- The voltage V_G(x) between the metal gate and the channel changes along the channel as:

$$V_G(x) = V_{GS} - \Psi(x)$$

$\Psi(x=0)$ = 0 V
$\Psi(x=L)$ = V_{DS}

- Consider the conducting channel as a lower electrode of a capacitor with SiO_2 dielectric and a metal gate as an upper electrode.
- V_G(x) - V_{Tn} voltage induces a charge per unit area in the channel Q_{invn}:

$$Q_{invn} = -C_{ox} \cdot [V_G(x) - V_{Tn}] = -q\int_{-\infty}^{0} n(x,y)dy \quad \left[\frac{A \cdot s}{m^2}\right]$$

Crude approximation!

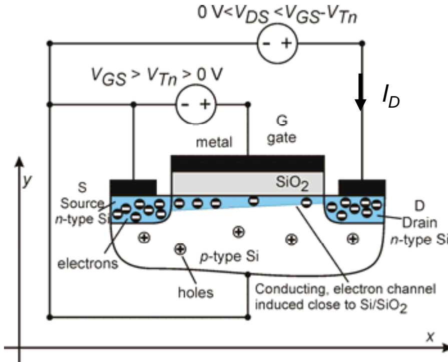
$$Q_{invn} = -C_{ox} \cdot [V_{GS} - V_{Tn} - \Psi(x)] \quad \left[\frac{A \cdot s}{m^2}\right]$$

where $C_{ox} = \frac{\varepsilon_{SiO2}\varepsilon_0}{t_{ox}}$

t_{ox} – gate oxide thickness
ε_{SiO2} ε_0 – dielectric constant of SiO_2

Drain current in triode (linear, nonsaturation) area

$V_{GS} > V_{Tn}$, $0\ V < V_{DS} < V_{GS} - V_{Tn}$



- We use the expression for the charge of electrons per unit area in the channel Q_{invn}:

$$Q_{invn} = -C_{ox} \cdot [V_{GS} - V_{Tn} - \Psi(x)]$$

- and expression for current in a thin layer I_{nx}

$$I_D = -WQ_{invn}\mu_n \mathscr{E}_x$$

- This yields the increment of potential at a small distance of dx

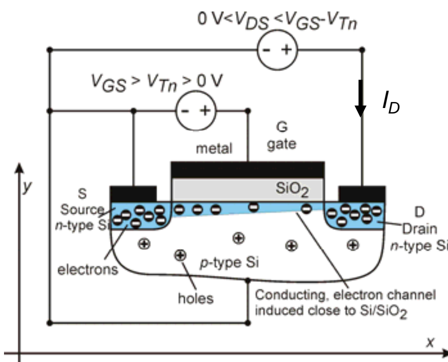
$$d\Psi(x) = \frac{I_D \cdot dx}{\mu_n W C_{ox} \cdot [V_{GS} - V_{Tn} - \Psi(x)]}$$

$$\int_0^{VDS} \mu_n W C_{ox} \cdot [V_{GS} - V_{Tn} - \Psi] \cdot d\Psi = \int_0^L I_D \cdot dx$$

where $C_{ox} = \dfrac{\varepsilon_{SiO2}\varepsilon_0}{t_{ox}}$

Drain current in triode (linear, nonsaturation) area

$V_{GS} > V_{Tn}$, $0\ V < V_{DS} < V_{GS} - V_{Tn}$



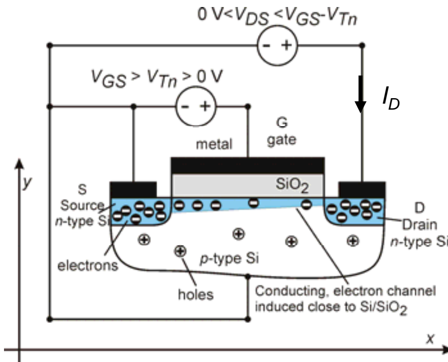
- Drain current intensity is constant at the entire channel length.

$$\mu_n W C_{ox} \cdot \int_0^{VDS} [V_{GS} - V_{Tn} - \Psi] \cdot d\Psi = I_D \cdot \int_0^L dx$$

gdzie $C_{ox} = \dfrac{\varepsilon_{SiO2}\varepsilon_0}{t_{ox}}$

- After integration we obtain expression for $I_D(V_{DS}, V_{GS})$

Drain current in triode (linear, nonsaturation) area



- Expression for static characteristics of a MOS field effect transistor $I_D(V_{DS}, V_{GS})$:
  (A crude approximation!)

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left[(V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

where $C_{ox} = \dfrac{\varepsilon_{SiO2}\varepsilon_0}{t_{ox}}$

- It holds for the following range of V_{DS} i V_{GS}

$V_{GS} > V_{Tn}$

$0\text{ V} < V_{DS} < V_{GS} - V_{Tn}$

- At this range of V_{DS} values the V_{GS} voltage is large enough to invert the channel at its entire length.
- For the larger V_{DS} values the inversion layer is not induced on the drain side of the channel.

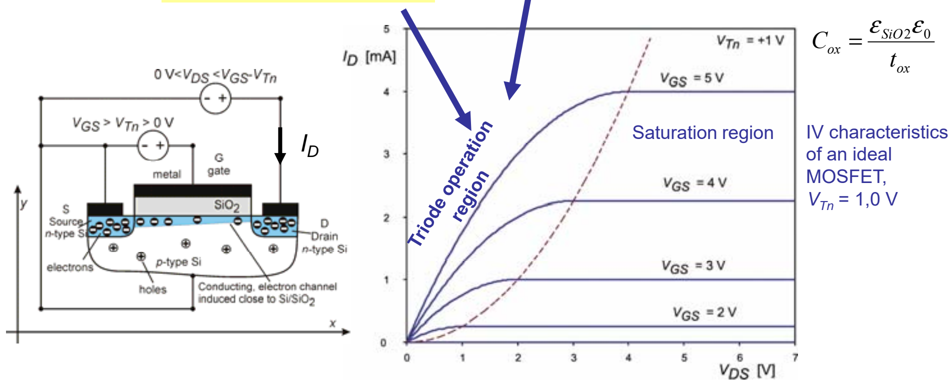
Drain current in triode (linear, nonsaturation) area

- For the V_{DS} i V_{GS} voltages of

$V_{GS} > V_{Tn}$

$0\text{ V} < V_{DS} < V_{GS} - V_{Tn}$

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \left[(V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$



$C_{ox} = \dfrac{\varepsilon_{SiO2}\varepsilon_0}{t_{ox}}$

IV characteristics of an ideal MOSFET, V_{Tn} = 1,0 V

- A single $I_D(V_{DS})$ curve at a fixed V_{GS} has a shape of a an inverted parabola with a maximum at $V_{DS}=V_{GS}-V_{Tn}$ – that is at the limit of applicability.
- This operation area is refered to as a triode area or linear or nonsaturation or non-pinch-off operation area of a MOS transistor.

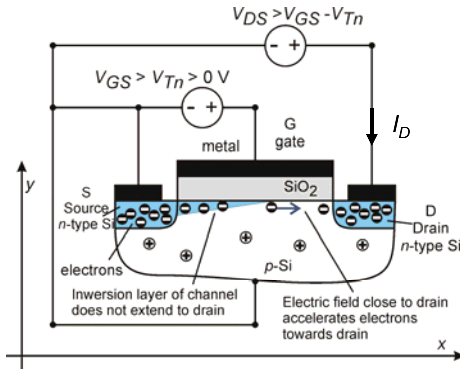
Prąd drenu w obszarze nasyc - 1

Drain current in saturation (pentode, pinch-off) area

- For the higher V_{DS} voltages, when

$V_{GS} > V_{Tn}$

$V_{DS} > V_{GS} - V_{Tn}$



- Inversion layer of the n type channel is induced only under a part of the gate SiO_2 – near the source.
- The drain current I_D flows.
- The drain current I_D for a given value of V_{GS} is equal to the maximum value of I_D at a triode area :

$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \frac{(V_{GS} - V_{Tn})^2}{2}$$

- The drain current I_D depends only on V_{GS} and is independent of the V_{DS} value.
- *IV* curves of MOSFETs in modern integrated circuits differ from this simple model.

- This operation area is refered to as a saturation area or pentode or pinch-off operation area of a MOS transistor.

Output IV characteristics of idealized MOSFET with induced *n*-channel

- For triode operation region, when

$V_{GS} > V_{Tn}$

$0\ V < V_{DS} < V_{GS} - V_{Tn}$

$$I_D = \beta_n \cdot \left[(V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- For saturation region, when

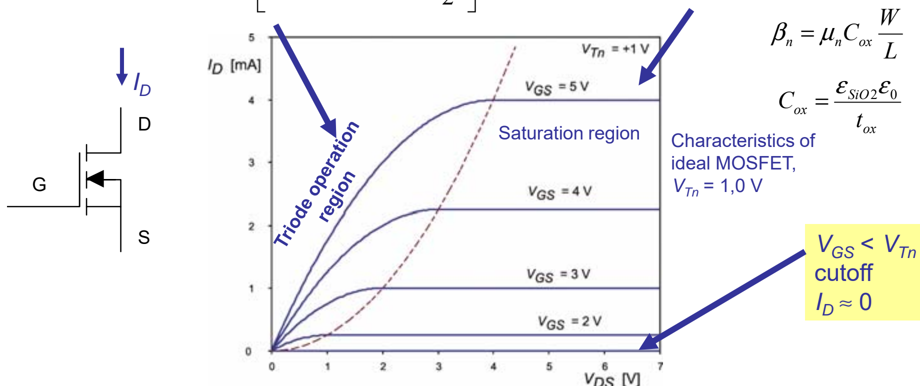
$V_{GS} > V_{Tn}$

$V_{DS} > V_{GS} - V_{Tn} > 0\ V$

$$I_D = \beta_n \cdot \frac{(V_{GS} - V_{Tn})^2}{2}$$

$$\beta_n = \mu_n C_{ox} \frac{W}{L}$$

$$C_{ox} = \frac{\varepsilon_{SiO2} \varepsilon_0}{t_{ox}}$$



$V_{GS} < V_{Tn}$
cutoff
$I_D \approx 0$

- Characteristics of modern MOSFETs in integrated circuits differ from this model.
- It can be used, however, as a coarse approximation for designing new circuits.

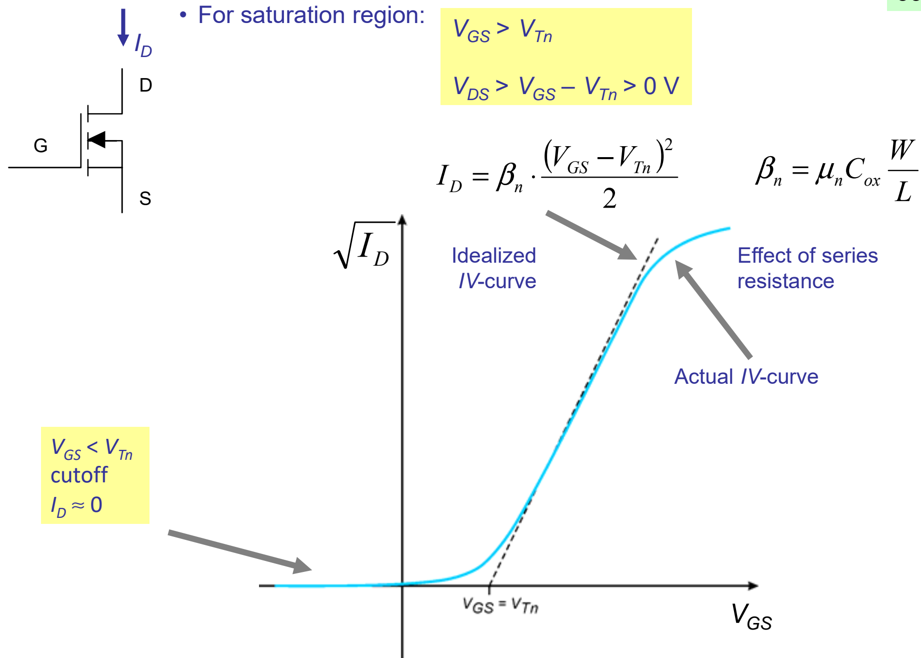
Transfer characteristics of MOSFET with induced *n*-channel

- For saturation region:

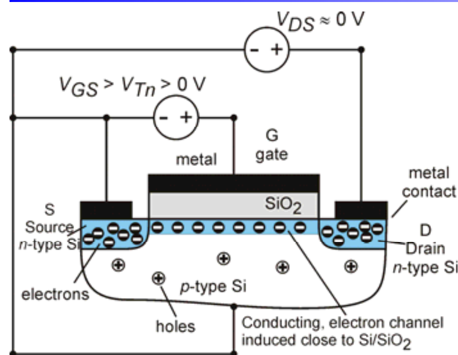
$V_{GS} > V_{Tn}$

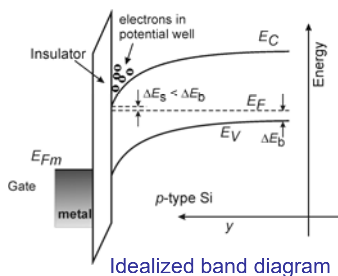
$V_{DS} > V_{GS} - V_{Tn} > 0$ V

$$I_D = \beta_n \cdot \frac{(V_{GS} - V_{Tn})^2}{2} \qquad \beta_n = \mu_n C_{ox} \frac{W}{L}$$



Threshold voltage V_{Tn} of MOSFET with induced *n*-channel





Idealized band diagram

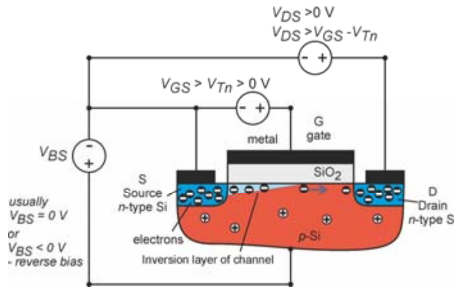
- Si under SiO_2 interface in a state of strong inversion - „band bending" of $2\Phi_{FBulk}$,
- which results in a voltage drop across the gate oxide of the value of :

$$-Q_B/C_{ox}$$

- where Q_B – electrical charge of ionized acceptor atoms in the deletion layer under the gate oxide.
- Effect of metal-semiconductor work-function difference Φ_{ms};
- Effect of electrical charge trapped at the oxide-semiconductor interface and at the gate oxide Q_f :

$$V_{Tn0} \approx \Phi_{ms} - \frac{Q_f}{C_{ox}} + 2\Phi_{FBulk} - \frac{Q_B}{C_{ox}}$$

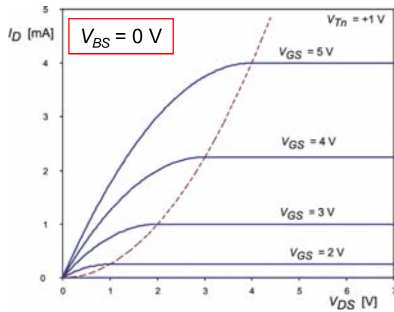
Effect of V_{BS} - bulk-source (substrate-source) potential difference

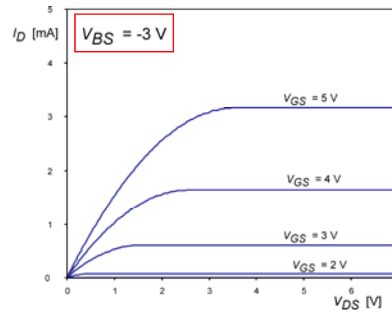


- Application of nonzero bulk-source voltage, $V_{BS} \neq 0$, results in a changed thickness of a depletion layer under the gate.
- This leads to a change in the total electrical charge of ionized acceptors in the depletion layer, which in turn affects the value of V_{Tn} .
- The substrate (bulk) may be used as an additional gate for the drain current control, but its efficiency – related transconductance - is small.

Modeling of V_{BS} effect in SPICE program:

$$V_{Tn} \approx V_{Tn0} + \gamma\left(\sqrt{2\Phi_{FBulk} - V_{BS}} - \sqrt{2\Phi_{FBulk}}\right)$$





Effect of high intensity electric field $\mathscr{E}$ in a channel

For high intensities of electric field $\mathscr{E}$, in silicon $\mathscr{E} > 10^4$ V/cm, drift velcities of electrons and holes reach the saturation values $v_{driftn} \approx v_{driftp} \approx v_{sat} \approx 10^7$ cm/s. It happens in modern transistors of short channels.

In the pentode area

Assuming that μ_n = const.

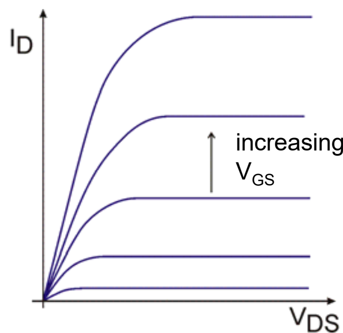
$$I_D = \mu_n C_{ox} \frac{W}{L} \cdot \frac{(V_{GS} - V_{Tn})^2}{2}$$

Quadratic dependence of I_D on V_{GS} .

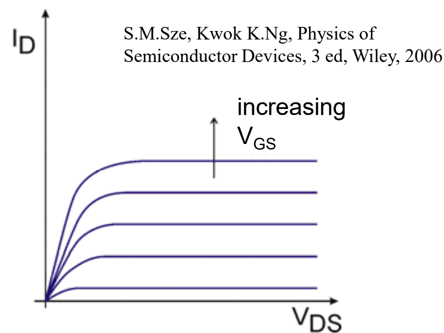
Assuming that $v_{driftn} \approx v_{sat}$

$$I_D = v_{sat} C_{ox} W (V_{GS} - V_{Tn})$$

Linear dependence of I_D on V_{GS} .



S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006



2nd Generation 32-nm High-k + Metal Gate Transistors - Intel 2010

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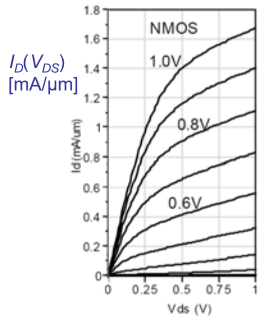
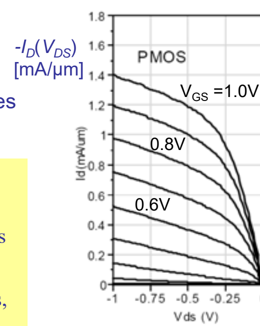
n-channel MOS transistor. *p*-channel MOS transistor.



$I_D(V_{DS})$ [mA/μm]

Channel length L = 32 nm.

$I_D(V_{DS})$ characteristics for fixed V_{GS} values



$-I_D(V_{DS})$ [mA/μm]

- Drain current $|I_D|$ does not increase with $|V_{GS}|$ square.
- V_{DS} has significant influence on I_D that is $r_{DS} \neq \infty$.
- These are results of short channel lengths, 32 nm.

Assume V_{DS} = 0,5 V and let us estimate the electric field intensity $\mathscr{E}$:

$$\mathscr{E} \approx \frac{0{,}5\text{V}}{32\text{nm}} \approx 1{,}5 \cdot 10^5 \ \text{V/cm}$$

$\mathscr{E} > 10^4$ V/cm, therefore, the drift velocities of electrons and holes approach the sauration values: $v_{driftn} \approx v_{driftp} \approx v_{sat} \approx 10^7$ cm/s.

$$I_D = v_{sat} C_{ox} W (V_{GS} - V_{Tn})$$

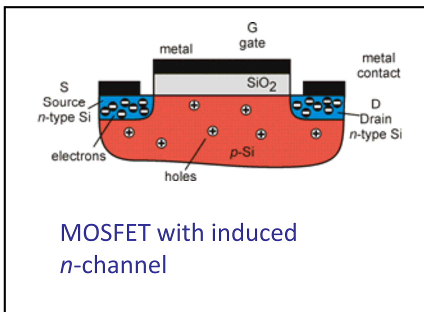
This is the reason for nearly proportional dependence of I_D on V_{GS} .

P. Packan i in., IEDM 2009 ss.659-662

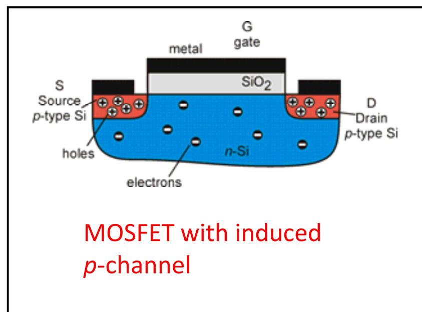
nMOS i pMOS - 1

nMOSFET i pMOSFET – comparison of output IV characteristics

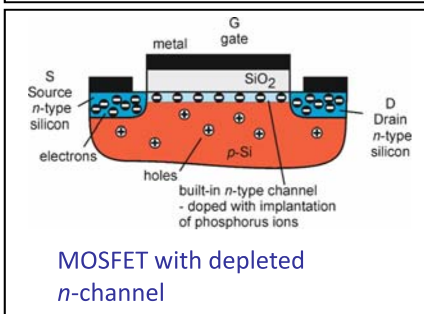
58



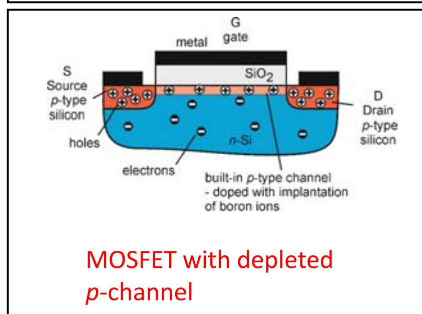
MOSFET with induced *n*-channel



MOSFET with induced *p*-channel

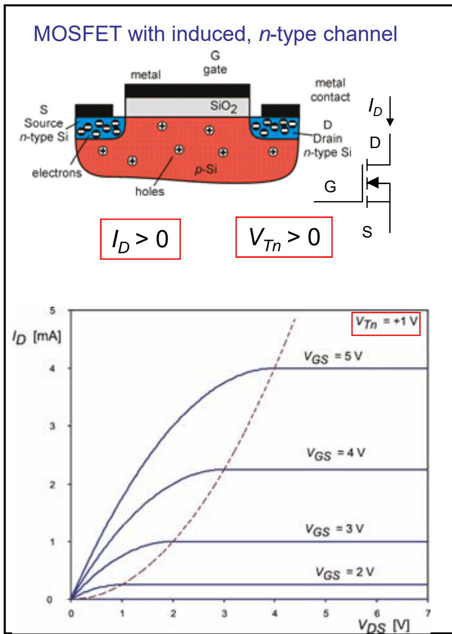


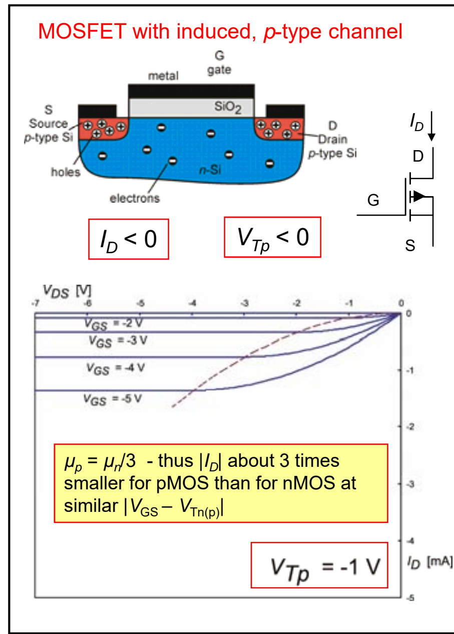
MOSFET with depleted *n*-channel



MOSFET with depleted *p*-channel

nMOSFET i pMOSFET – comparison of output IV characteristics





nMOSFET i pMOSFET – comparison of IV characteristics

MOSFET with induced, n-type channel

cut-off area: $V_{GS} <= V_{Tn}$

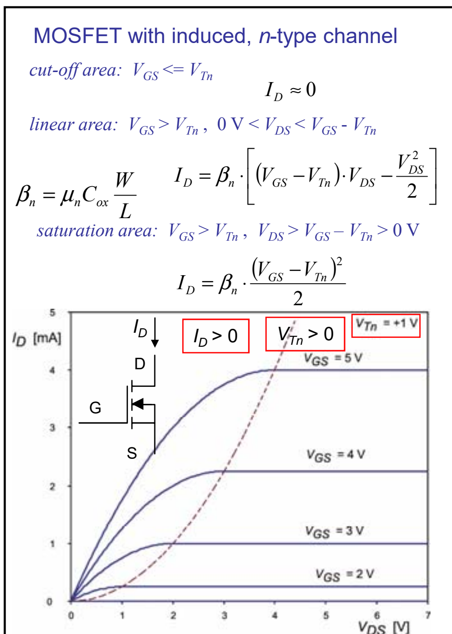
$$I_D \approx 0$$

linear area: $V_{GS} > V_{Tn}$, $0\text{ V} < V_{DS} < V_{GS} - V_{Tn}$

$$\beta_n = \mu_n C_{ox} \frac{W}{L} \qquad I_D = \beta_n \cdot \left[(V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

saturation area: $V_{GS} > V_{Tn}$, $V_{DS} > V_{GS} - V_{Tn} > 0\text{ V}$

$$I_D = \beta_n \cdot \frac{(V_{GS} - V_{Tn})^2}{2}$$



MOSFET with induced, p-type channel

cut-off area: $V_{GS} >= V_{Tp}$

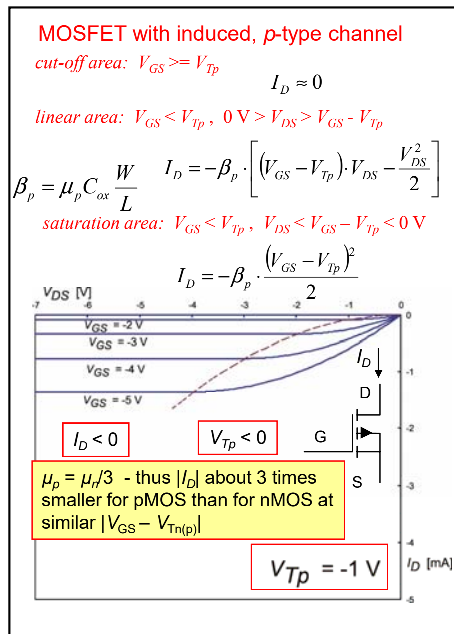
$$I_D \approx 0$$

linear area: $V_{GS} < V_{Tp}$, $0\text{ V} > V_{DS} > V_{GS} - V_{Tp}$

$$\beta_p = \mu_p C_{ox} \frac{W}{L} \qquad I_D = -\beta_p \cdot \left[(V_{GS} - V_{Tp}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

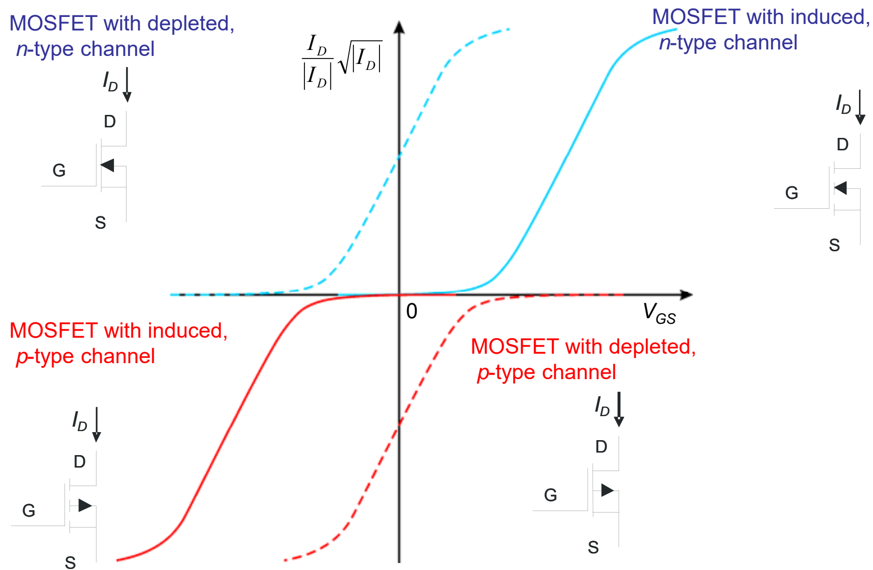
saturation area: $V_{GS} < V_{Tp}$, $V_{DS} < V_{GS} - V_{Tp} < 0\text{ V}$

$$I_D = -\beta_p \cdot \frac{(V_{GS} - V_{Tp})^2}{2}$$

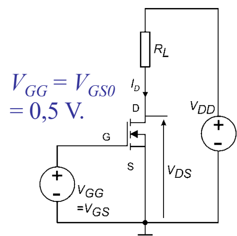


nMOS i pMOS - 4

nMOSFET i pMOSFET – comparison of transfer IV characteristics



A direct-current operation point of a MOS transistor



For a transistor of known characteristics we want to find DC current and voltages $V_{GG} = V_{GS0} = 0{,}5$ V.

We solve the set of two equations:

$$I_D(V_{DS}, V_{GS}) = f(V_{DS}, V_{GS})$$ - equation of static characteristics of the transistor

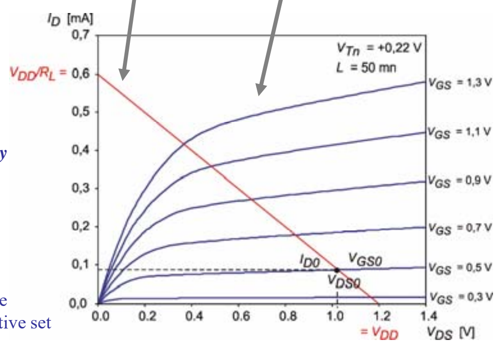
$$V_{DS} + I_D R_L = V_{DD}$$ - equation of the load line

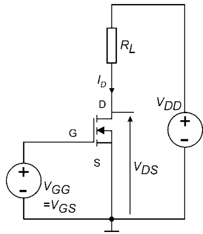
Note:

The characteristics of transistors are usually described withdifferent forms of the equations for cut-off, triode-, and pentode-regions of operation.

For finding the DC operation point (I_{D0}, V_{DS0}, V_{GS0}) by solving equations it is convenient to:

- assume that the transitor operates for instance at the saturation region,
- solve the set of the respective set of the equations,
- verify the applicability of the assumption,
- if the applicability was not confirmed then change the assumed operation region and again solve the respective set of equations..

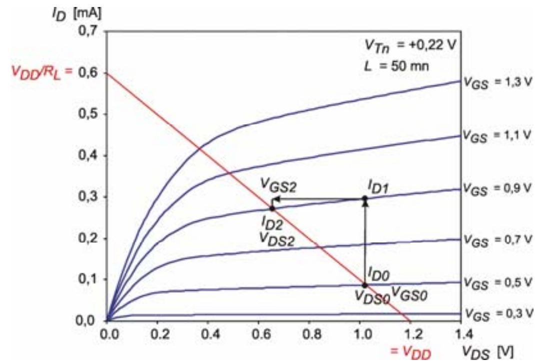




Suppose that in the beginning $V_{GG} = V_{GS0} = 0{,}5$ V.

Suppose also that V_{GS} is varied: $V_{GS2} = V_{GS0} + \Delta V_{GS}$.

Let us find: I_{D2} , V_{GS2}.



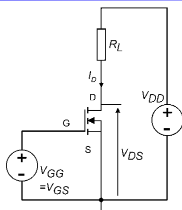
$$\Delta I_D = I_{D2} - I_{D0}$$

$$\Delta I_D = (I_{D1} - I_{D0}) + (I_{D2} - I_{D1})$$

$$I_{D1} - I_{D0} \approx \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS=const.} \cdot \Delta V_{GS}$$

$$I_{D2} - I_{D1} \approx \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{VGS=const.} \cdot \Delta V_{DS}$$

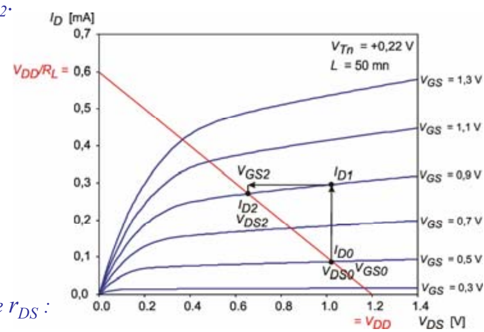
$$\Delta I_D \approx \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS=const.} \cdot \Delta V_{GS} + \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{VGS=const.} \cdot \Delta V_{DS}$$



Suppose that in the beginning $V_{GG} = V_{GS0} = 0{,}5$ V.

Suppose also that V_{GS} is varied: $V_{GS2} = V_{GS0} + \Delta V_{GS}$.

Let us find: I_{D2} , V_{GS2}.



$$\Delta I_D \approx \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS=const.} \cdot \Delta V_{GS} + \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{VGS=const.} \cdot \Delta V_{DS}$$

Let us define transconductance g_m:

$$g_m \approx \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS=const.}$$

Let us define output conductance g_{DS} and resistance r_{DS} :

$$g_{DS} = \frac{1}{r_{DS}} \approx \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{VGS=const.}$$

Therefore: $\Delta I_D \approx g_m \cdot \Delta V_{GS} + g_{DS} \cdot \Delta V_{DS}$

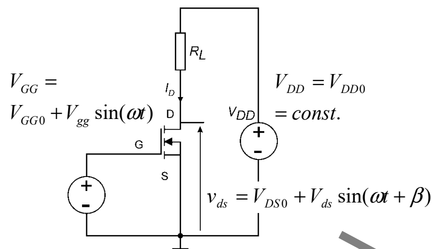
And, using the load line equation: $\Delta V_{DS} = -R_L \cdot \Delta I_D$

Finally:

$$\Delta I_D \approx \frac{g_m r_{DS}}{r_{DS} + R_L} \cdot \Delta V_{GS}$$

$$\Delta V_{DS} \approx -\frac{g_m r_{DS} R_L}{r_{DS} + R_L} \cdot \Delta V_{GS}$$

$i_d = I_{D0} + I_d \sin(\omega t + \alpha)$

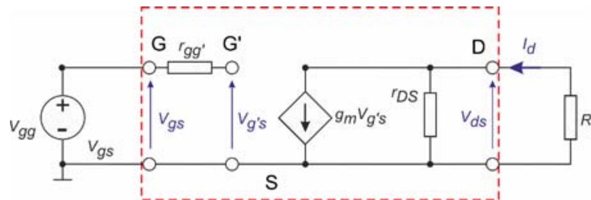


Calculated amplitudes of small-signal components:

$$I_d \approx \frac{g_m r_{ds}}{r_{ds} + R_L} \cdot V_{gs} \quad \text{where} \quad r_{ds} \approx r_{DS}$$

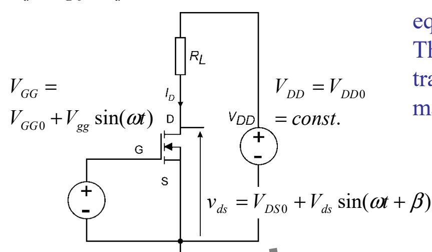
$$V_{ds} \approx -\frac{g_m r_{ds} R_L}{r_{ds} + R_L} \cdot V_{gs}$$

It is to note , that exactly the same, linear dependencies between the AC components of currents and voltages are obtained for the circuit as below.



We have thus linearized the characteristics of our transistor in the process of solving for the response of the circuit at small-signal variation of some voltage close to the DC operation point *(I_{D0}, V_{DS0}, V_{GS0}).*

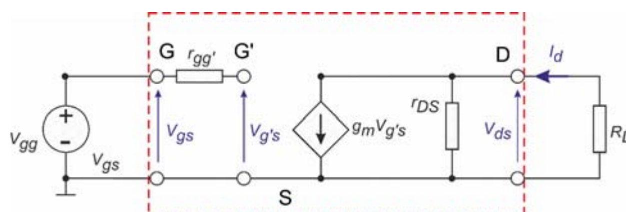
$i_d = I_{D0} + I_d \sin(\omega t + \alpha)$



This linearized circuit is called a small-signal equivalent circuit..
The small-signal equivalent circuit of a MOS transistor in a common source configuration is marked with a red envelope line below.

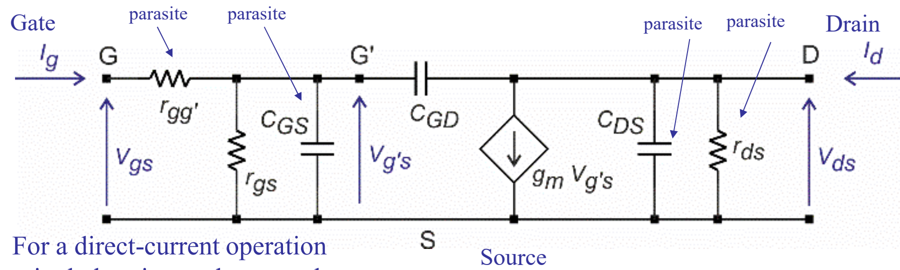
Method of obtaining the small signal equivalent circuit :

- substitute the independent voltage sources in the real circuit with conductor lines (short-circuits);
- substitute the independent current sources in the real circuit with openings (open-circuits);
- substitute the transistors with their small-signal equivalent circuits.



Small-signal transistor equivalent circuit for medium frequencies 67

- including gate-source capacitances C_{GS} and gate-drain capacitances C_{GD}, as well as parasitic elements



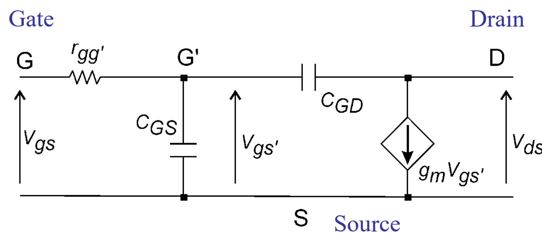
For a direct-current operation point belonging to the pentode region:

$$C_{GS} \approx \frac{1}{2} WL \cdot C_{ox}$$

$$C_{GD} < \frac{1}{2} WL \cdot C_{ox}$$

The capacitances account for the electric charges of the flowing carriers and, also, for the charges stored in the depletion layer under the gate oxide.

Cut-off frequencies for operation with small signals 68



Only the most important elements taken into account, including the series resistance of the gate, $r_{gg'}$.

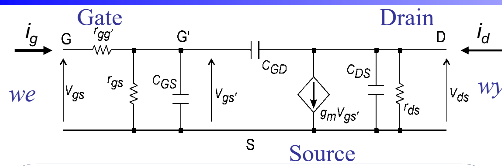
The current-gain cut-off frequency f_T of a MOS transistor is the highest frequency at which the extrapolated current-gain of the transistor is not smaller than 1.

$$f_T \approx \frac{g_m}{2\pi WLC_{ox}} = \frac{g_m}{2\pi (C_{GS} + C_{GD})}$$

The power-gain cut-off frequency f_{max} of a MOS transistor is the highest frequency at which the extrapolated power-gain of the transistor is not smaller than 1.

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi \cdot r_{gg'} C_{GD}}}$$

Two-port network type models of a transistor



A small-signal eqiuvalent circuit of a transistors may be presented as a two-port network.
Source i shared by input and output – common source configuration.

$i_g = i_1$, $v_{gs} = v_1$
$i_d = i_2$, $v_{ds} = v_2$

$$V_{gs} = h_{11S} I_g + h_{12S} V_{ds}$$
$$I_d = h_{21S} I_g + h_{22S} V_{ds}$$

Hybrid-type equations

$$I_g = y_{11S} V_{gs} + y_{12S} V_{ds}$$
$$I_d = y_{21S} V_{gs} + y_{22S} V_{ds}$$

Admitance-type equations

$$V_{gs} = z_{11S} I_g + z_{12S} I_d$$
$$V_{ds} = z_{21S} I_g + z_{22S} I_d$$

Impedance-type equations

$[h_{ij}]$, $[y_{ij}]$ i $[z_{ij}]$ matrices are equivalent and may be transformed one into other one. At microwave frequencies it is convenient to use another equivalent matrices - $[S_{ij}]$ matrices.

Current gain:

$$h_{21S}(f) = \left.\frac{I_d(f)}{I_g(f)}\right|_{V_{ds}=0}$$

For field effect transistors we have:

$$f \to 0$$
$$\Rightarrow h_{21S}(f) \to \infty$$

Transconductance of a transistor:

$$g_m = y_{21S} = \left.\frac{I_d}{V_{gs}}\right|_{V_{ds}=0}$$

Record high current gain cut-off frequencies f_T of CMOS transistors fabricated in 45-nm technology - IBM 2007

Magnitude of current gain in a common-source configuration

$$\left|h_{21S}(f)\right| = \left|\frac{i_d(f)}{i_g(f)}\right|_{v_{ds}=0}$$

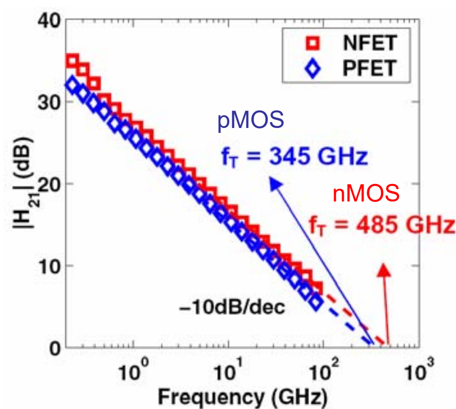
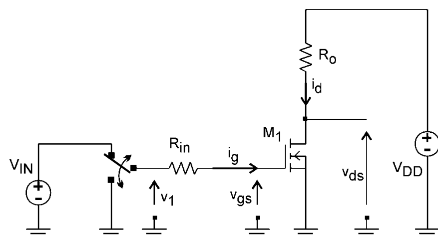


Fig. 2. Current gain $|H_{21}|$ from measured S-parameters for 30 µm wide (1 µm by 30 gate fingers) SOI NFET (L_{poly} =29 nm) and SOI PFET (L_{poly} =31 nm) with relaxed poly pitch at V_{GS} = 0.6 (-0.6) V, V_{DS} =1.0 (-1.0) V.

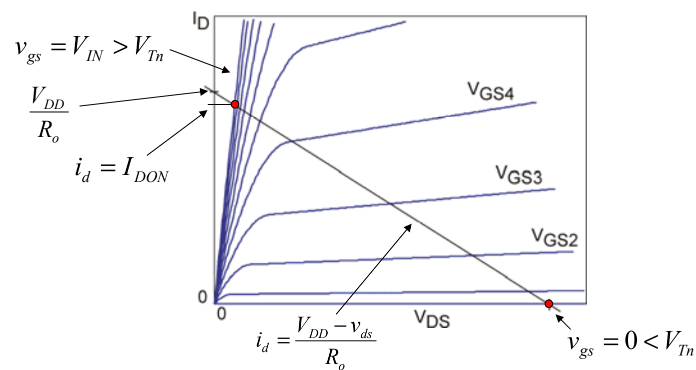
IEDM 2007, art. s10p04, IBM

Nonlinear operation of MOS transistor in a pulse circuit

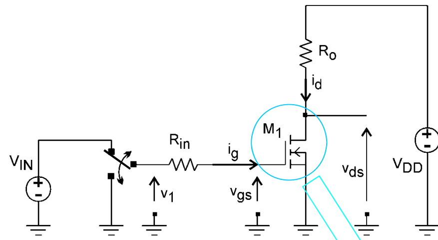
Operation of MOS transistor in a pulse circuit



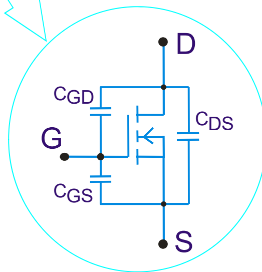
Zmiana napięcia v_{gs} powoduje zmianę prądu drenu i_d oraz napięcia v_{ds}. Punkt pracy przesuwa się wzdłuż prostej obciążenia ze zwłoką wynikającą z ładowania pojemności tranzystora przez prądy o ograniczonych wartościach.



Operation of MOS transistor in a pulse circuit



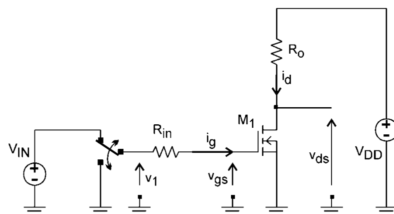
Changing v_{gs} leads to varying i_d current and v_{ds} voltage. The operation point is being shifted along the load line. The delay of this process is due to charging of the capacitances of the transistor with currents of limited values.



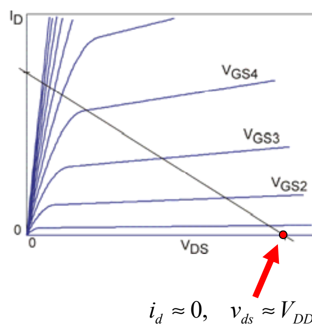
Hypothetic inertion-less trasistor with added external capacitors.

MOS_switch_2

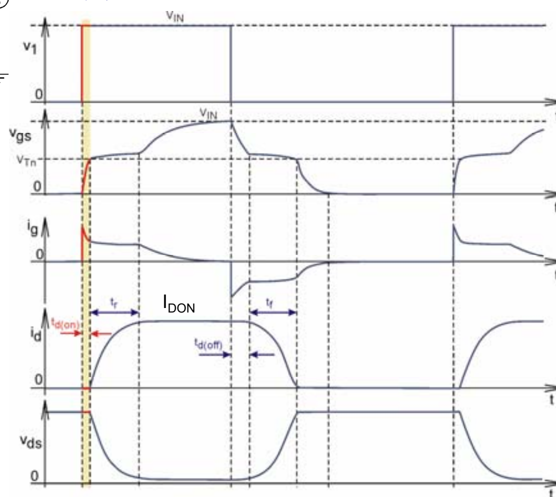
Operation of MOS transistor in a pulse circuit



- R_{in} lead is switched from ground to V_{IN}.
- $v_{gs}<V_{Tn}$ - C_{gs} capacitance being charged from 0 V to V_{Tn}.
- $i_d \approx 0$ for time shorter than $t_{d(ON)}$ from the pulse edge *($t_{d(ON)}$ – turn-on delay time)*.



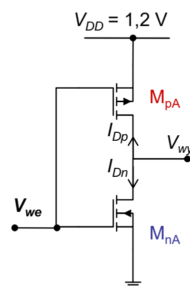
$$i_d \approx 0, \quad v_{ds} \approx V_{DD}$$

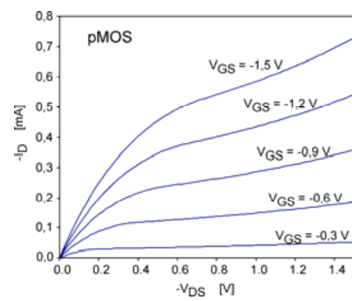


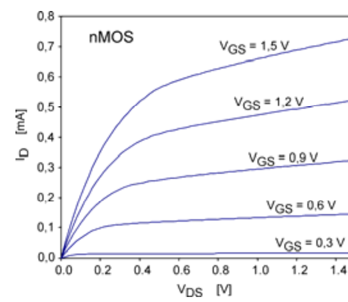
MOS_switch_3

CMOS inverter
– a basic CMOS gate

Example CMOS inverter with transistors of 50-nm channels







Graphical method of transfer *IV* characteristic of CMOS inverter determination

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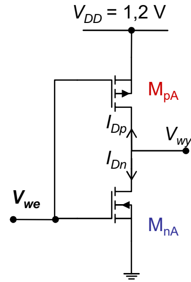
pMOS transistor serves as load for nMOS (and oppositely

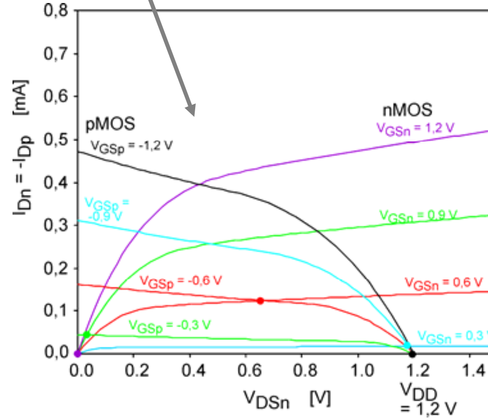
$I_{Dn} = - I_{Dp}$

$V_{DSn} = V_{DD} + V_{DSp}$

$V_{GSp} = V_{GSn} - V_{DD}$

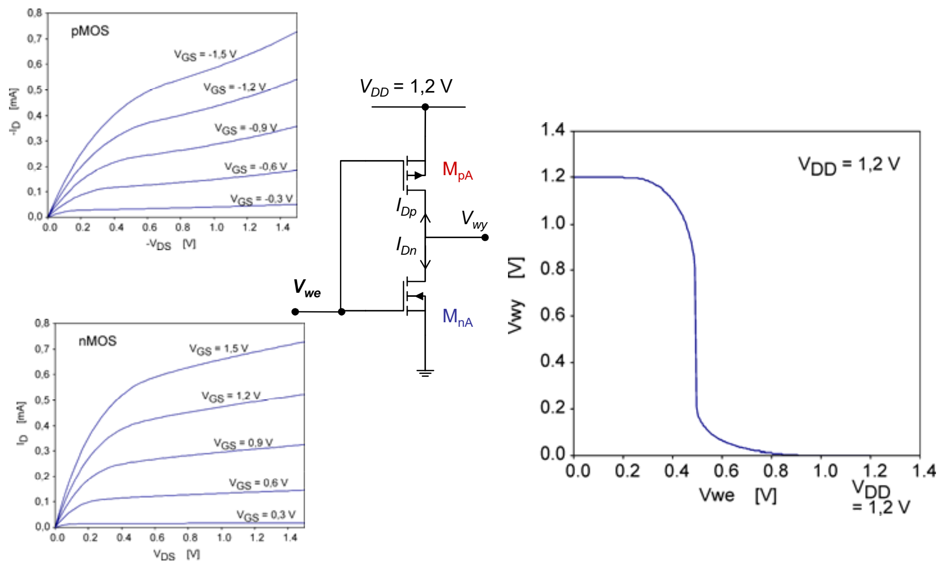


Corresponding pairs of characteristics for nMOS and pMOS transistors plotted with the same colors.

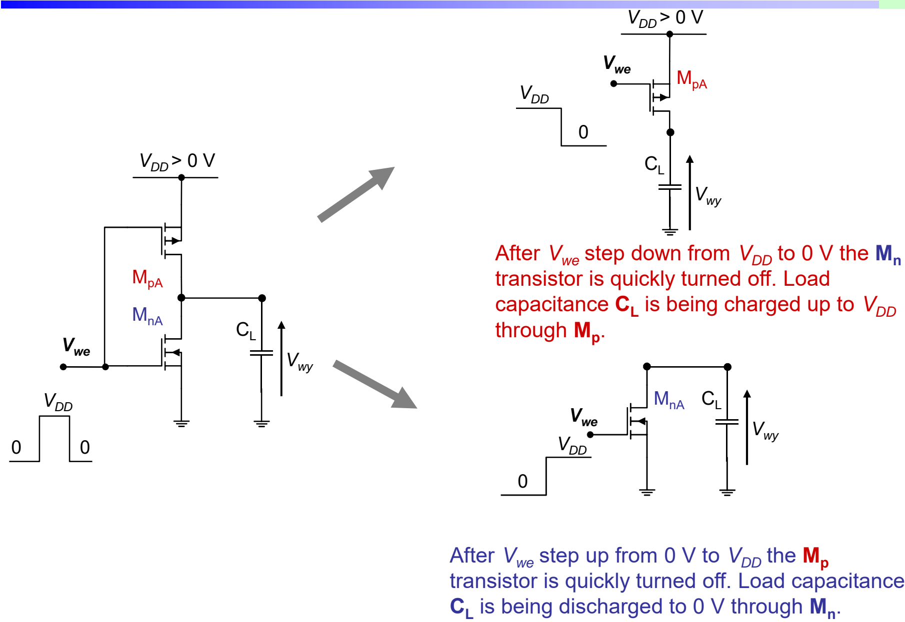


Static transfer characteristic for CMOS inverter is usually calculated numerically

78



Pulse operation of CMOS inverter



Power loss at CMOS inverter

$$P_{tot} = C_L \cdot V_{DD}^2 \cdot f + I_G\big|_{VGS=VDD} \cdot V_{DD} + I_D\big|_{VGS=0} \cdot V_{DD}$$

Power loss for charging and discharging of load capacitance C_L

Power loss for gate dielectric conduction (tunnelig current).

Power loss for D-S DC leakage

- In older CMOS circuits power was consumed mainly for charging and discharging capacitancies C_L of subcircuits.
- Few years ago, for gate dielectric layers thinner than 5 nm, power loss resulting from tunneling currents in gate dielectrics become considerable.
- Few years ago, for channel lengths L smaller than 50 nm, power loss resulting D-S leakage become considerable.

Scaling down field effect transistors in CMOS integrated circuits

30 Years of CMOS Scaling 1978 - 2008

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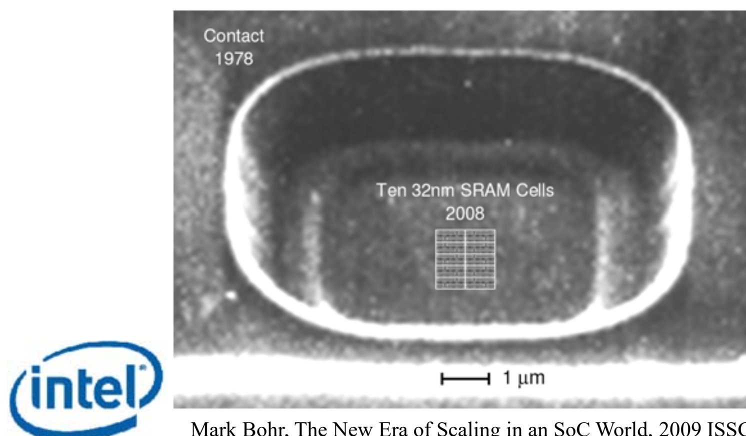
- Device operation speed is limited by a path length and velocity of electrons.

$$f_{cutoff} \le \frac{l_{transit}}{2\pi v_{transit}}$$

- Number of logic gates per unit area increases as the size of device decreases.

$$\frac{N}{Area} \propto l_{\min}^2$$



Mark Bohr, The New Era of Scaling in an SoC World, 2009 ISSCC

Scaling coefficients of CMOS transistors at conservation of fixed electrical field intensities and power density

83

	Parametr	Scaling coefficient	Parameter
We change	Rozmiar (t_{ox}, r_j, W, L)	λ^{-1}	Dimension (t_{ox}, r_j, W, L)
	Napięcie zasilania (V_{DD})	λ^{-1}	Supply voltage (V_{DD})
	Napięcie progowe (V_{Tn}, V_{Tp})	λ^{-1}	Threshold voltage (V_{Tn}, V_{Tp})
	Koncentracje domieszek (N_A, N_D)	λ	Dopant concentrations (N_A, N_D)
We obtain	Pojemność charakt. bramki (C_{ox})	λ	Specific gate capacitance (C_{ox})
	Pojemność bramki (C_G)	λ^{-1}	Gate capacitance (C_G)
	Prąd drenu (I_D)	λ^{-1}	Drain current (I_D)
	Gęstość prądu (J)	λ	Current density (J)
	Moc zasilania (P)	λ^{-2}	Power consumption (P)
	Gęstość mocy (P/Area)	1	Power density (P/Area)
	Opóźnienie bramki (t_d)	λ^{-1}	Gate delay (t_d)
	Iloczyn moc·opóźnienie ($t_d \cdot P_g$)	λ^{-3}	Power-delay product ($t_d \cdot P_g$)
	Ilość tranzystorów na cm^2	λ^2	Integration density (transistors/cm^2)

P.K.K. Ko, "Approaches to scaling", Advanced MOS device physics, VLSI electronics microstructure science, Vol. 18, Academic Press, pp. 1-37, 1989

Changes in transistor size

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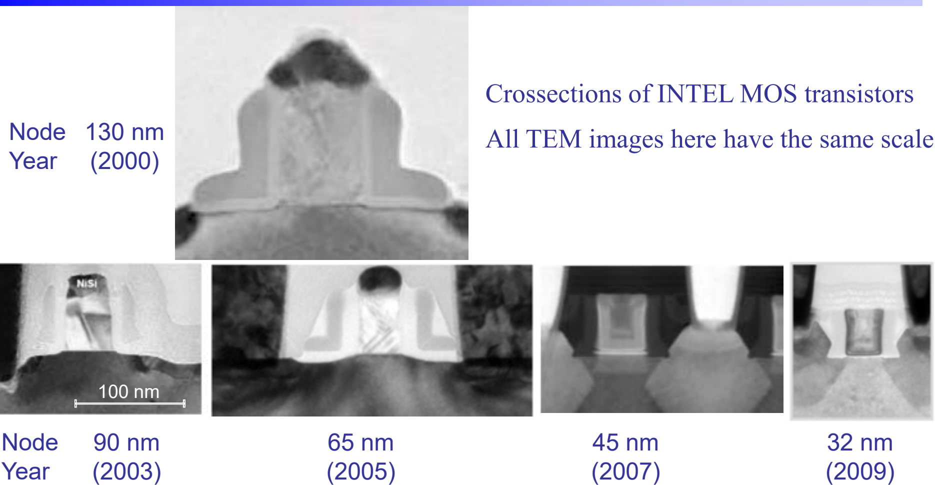
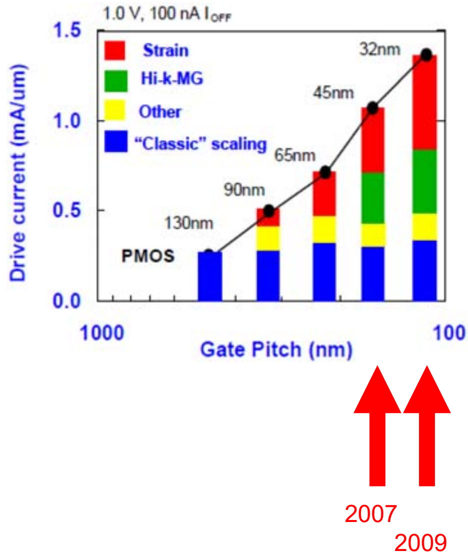


- Very little change in physical gate length, only ~0.9x per node
- The gate pitch is scaling fast, as 0.7x per node and area scales as 0.5x
- Most of the transistor innovation is in stress engineering and HKMG

K. Kuhn, CNNA, Berkeley 2010

V. Moroz, SYNOPSYS
Berkeley Seminar 2011

Influence of Si stress engineering, metal gate and high permittivity dielectric on speed of pMOSFET



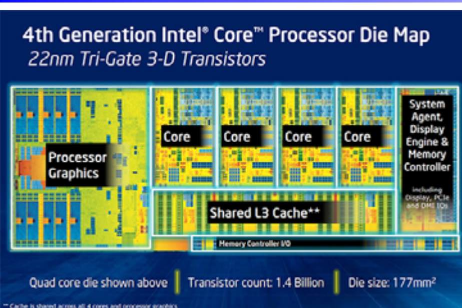
Conventional scaling rules fail.

Improvement of speed is obtained by increasing of drain current per unit length of channel width, which results from:

- intentionally introduced strain into Si;
- applying of metal gate and gate dielectric of high permittivity.

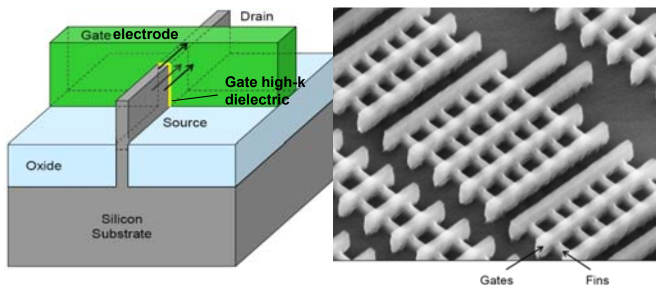
source: K. Kuhn et. al, ECS 2010 - Intel

2013 INTEL processor with „tri-gate" (FinFET) CMOS transistors



2013: Procesor Core i7-4770K (Haswell) with CMOS tri-gate (FinFET) transistors fabricated at a technology node of 22 nm.

source: Intel, 2013



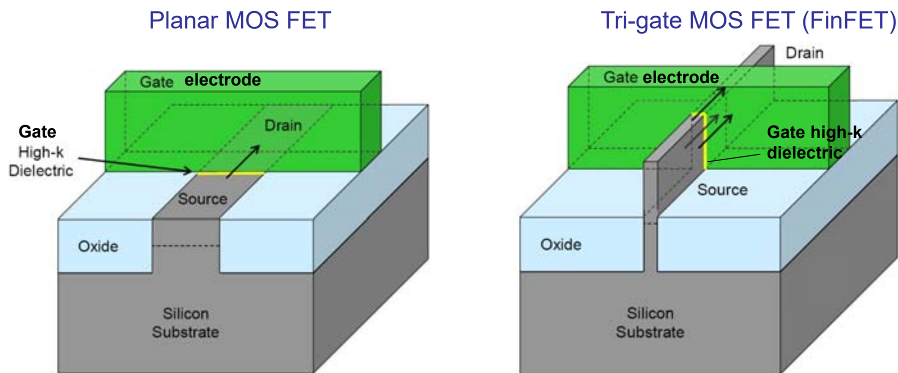
Sept. 2013:
Intel – 14-nm Broadwell Processor Consuming 30% Less Power Than 22nm Haswell

Oct. 07 2013:
TSMC – 16-nm FinFET technology to be presented in December at IEDM

source: M. Bohr, K. Mistry,
Intel's Revolutionary 22 nm Transistor Technology, May, 2011

Traditional planar MOS FET vs. tri-gate MOS FET (FinFET)

87



Traditional 2-D planar transistors form a conducting channel in the silicon region under the gate electrode when in the "on" state.

3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation.

source: M. Bohr, K. Mistry,
Intel's Revolutionary 22 nm Transistor Technology, May, 2011

Traditional planar MOS FET vs. tri-gate MOS FET (FinFET)

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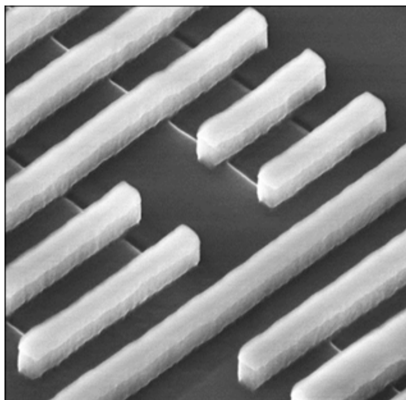
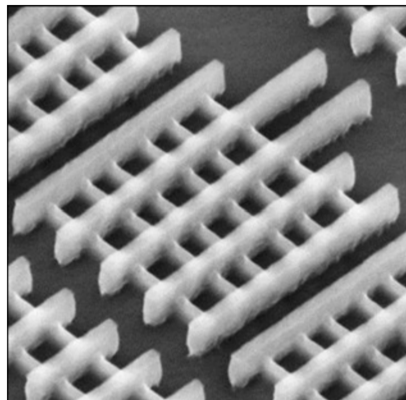
32 nm planar MOS FET

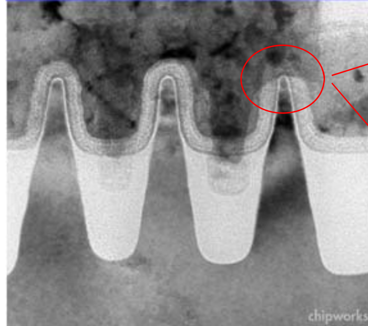


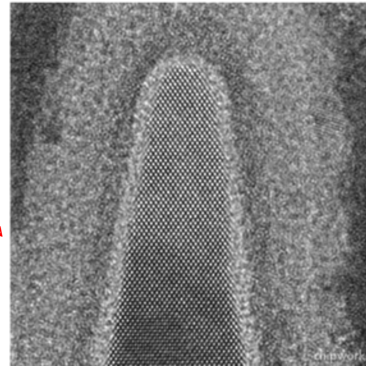
22 nm tri-gate MOS FET (FinFET)

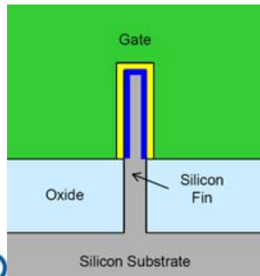


source: M. Bohr, K. Mistry,
Intel's Revolutionary 22 nm Transistor Technology, May, 2011

INTEL processor with fully depleted 22-nm tri-gate MOS FET (FinFET)







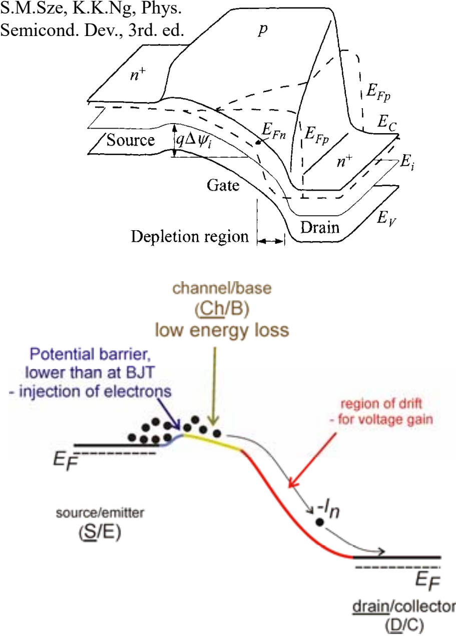
TEM Image of nMOS Gate and Fin Structure

source: Chris Auth, et. al., 2012 Symposium on VLSI Technology, Hawaii

Generic Idea of a Transistor -

(*Not quite*) A General Recipe for a Transistor

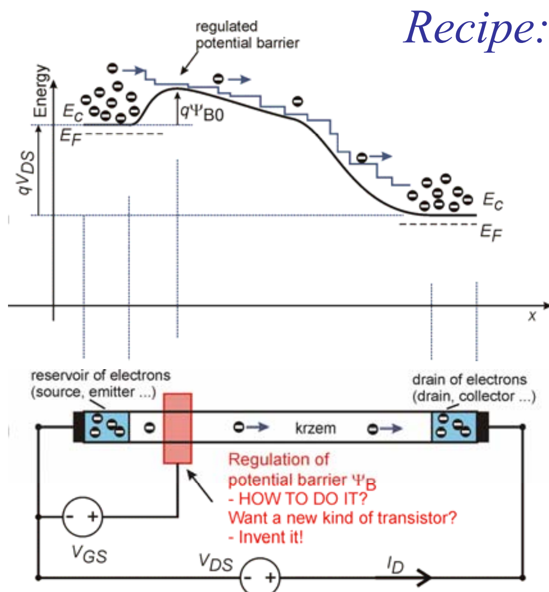
MOS field effect transistor



Our way of looking at the main current of a transistor may be applied to MOSFETs.

- Potential barrier is lower than for BJT,
- current is limited mainly by transport in the channel.

Want to make a new kind of a transistor – quite different?

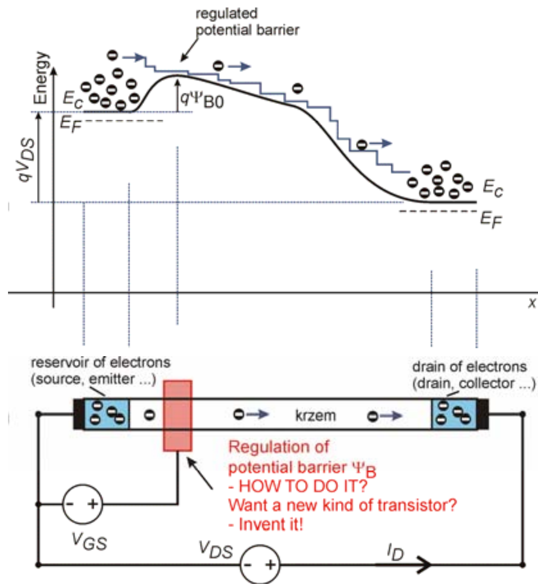


Recipe:

- Take a reservoir of electrons (source, emitter..).
- Take a second reservoir of electrons (drain, collector...) and put it at a lower energetic level – bias it positively with respect to the first one V_{DS}>0V.
- Insert a semiconductor of low n concentration between the source and the drain.
- Create in this region a potential barrier of Ψ_B height, which can be electrically regulated with changes of the control voltage V_{GS}.

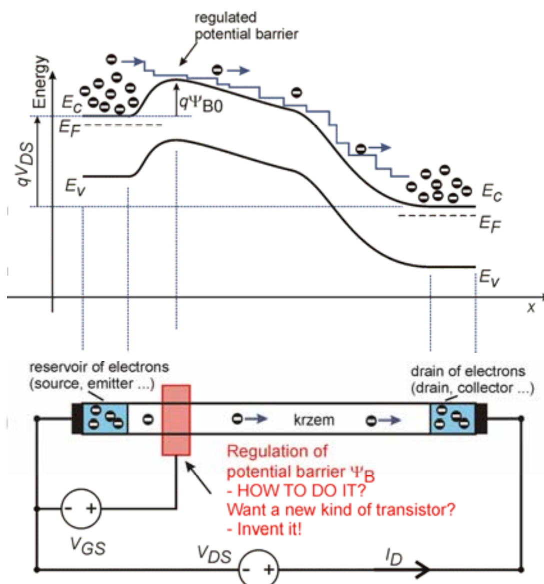
You have an useful transistor if you do it and obtain a power gain!

Effect of potential barrier on drain current



- Electrons in the 1st. reservoir, source, have different energies $E \geq E_c$. Probability of state occupation decreases strongly with increasing E.
- Electrons of higher energies contribute to overcome the barrier Ψ_B by some electrons.
- Electrons which managed to overcome the barrier Ψ_B drift in electric field $\mathscr{E}$ heading the 2nd. reservoir - drain. They create drain current I_D.
- Lowering of $|\Psi_B|$ results in increasing number of these electrons – Larger I_D flows.
- Increasing of $|\Psi_B|$ results in decreasing number of these electrons – Smaller I_D flows.

Band diagram for a transistor



- This is a diagram for a transistor made of one kind of a semiconductor (Si).
- Bandgap value

$$E_g = E_c - E_v$$

is constant in entire, transistor from source to drain.

- In general case different semiconductors, of different E_g values may be used for making different fragments of a transistor.

Possible mechanisms of electron and hole transport

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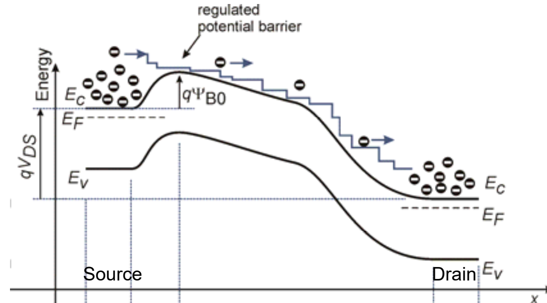
Diffusion and drift in electric field



Source-drain distances for transistors in mass production today are so large that electrons are many times scattered. Their energies and momenta relax.

Transport of carriers is described in terms of
diffusion
and drift in electric field $\mathscr{E}$ with averaged velocity.

Możliwe mechanizmy transportu dziur i elektronów -1

Possible mechanisms of electron and hole transport

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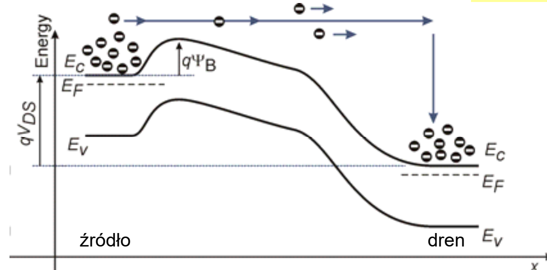
Możliwe mechanizmy transportu dziur i elektronów -2

Ballistic transport

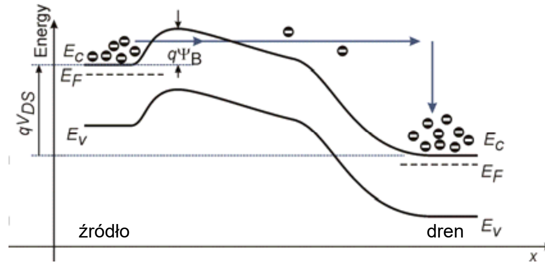


- Electrons are not scattered on a way from source to drain. Their energies and momenta do not relax.
- Their total energies do not change.
- Momentum of electron increases in $\mathscr{E}$ field, on a way from source to drain, so the kinetic energy increases too.
- Kinetic energy may be very high, transit time – very short.
- For GaAs the source-drain distance should be < 20 nm to avoid scattering, for silicon < 5 nm.
- These transistors could operate at $f > 10^{12}$ Hz ($f > 1$ THz)

Possible mechanisms of electron and hole transport

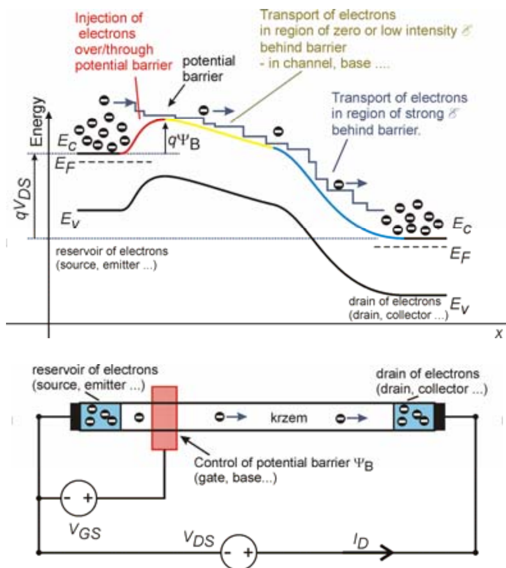
Możliwe mechanizmy transportu dziur i elektronów -3

Direct tunneling transport



- At very short source-drain distances probability of tunneling through the barrier becomes high.
- Tunneling current component exceeds ballistic component.
- This happens for GaAs transistors with source-drain distance of 10 nm.
- These transistors could also operate at $f > 10^{12}$ Hz ($f > 1$ THz)

Effects limiting the transistor current



- Transport of electrons in a region of low $\mathscr{E}$ in channel (behind potential barrier). This is a case of field effect transistors eg. MOS.
- Two effects together. Injection of electrons over potential barrier Ψ_B and also transport in a region of zero or low $\mathscr{E}$ inside base (behind potential barrier). This is a case of bipolar junction transistors.
- Injection of electrons over/through potential barrier Ψ_B. This is a case of transistors with very short channels. Ballistic or tunneling operation is expected.

Semiconductor Diodes

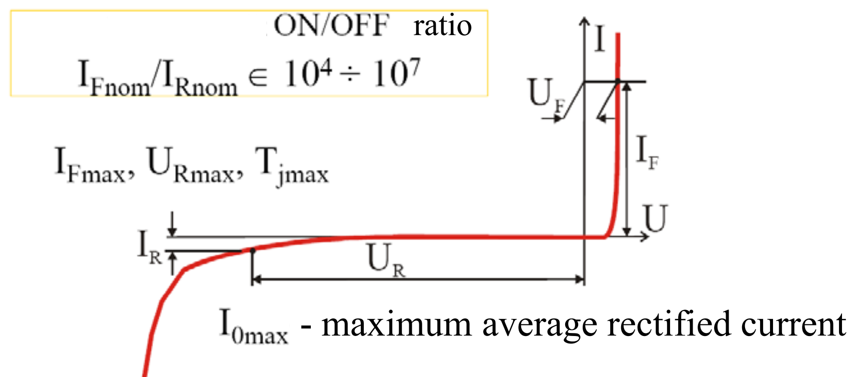
Diodes for rectifiers

A property that makes diodes useful for converting the AC current into direct current that is for rectifying is nonlinearity of its current-voltage characteristic.

ON/OFF ratio

$I_{Fnom}/I_{Rnom} \in 10^4 \div 10^7$

I_{Fmax}, U_{Rmax}, T_{jmax}



I_{0max} - maximum average rectified current

MPolowczyk_Diody prostownicze 2

Rys: Prof. dr hab. inż. M. Polowczyk

Silicon diodes in packages

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high power diodes

low power diodes

MPolowczyk_Diody prostownicze 3

Rys: Prof. dr hab. inż. M. Polowczyk

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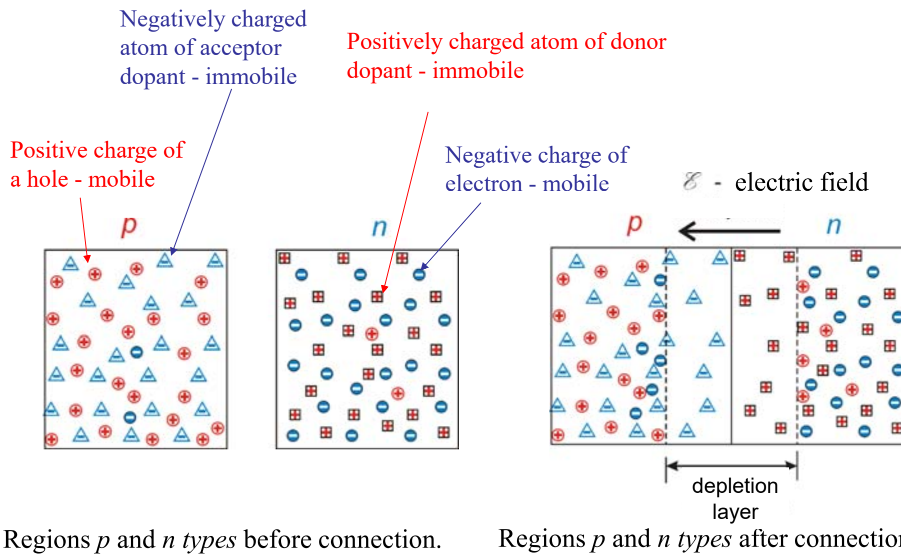
Semiconductor *pn* junction

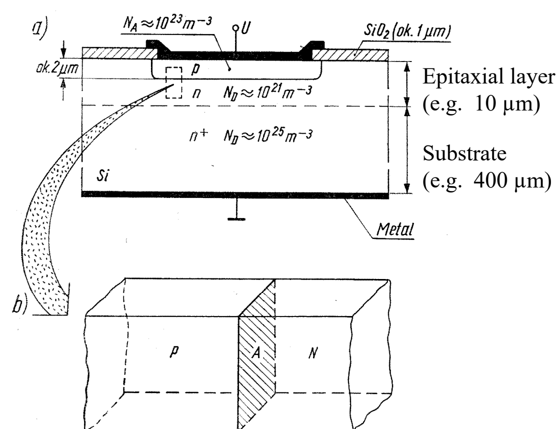
pn junction – schematic drawing of semiconductor structure



Regions *p* and *n types* before connection. Regions *p* and *n types* after connection.

rys: za W. Marciniak, Przyrządy półprzewodnikowe i układy scalone, WNT 1979

pn junction – cross-section of a chip



rys: W. Marciniak, Przyrządy półprzewodnikowe i układy scalone, WNT 1979

Workfunction is larger for *p*-type semiconductor than that for *n*-type semiconductor : $\Phi_{WFp} > \Phi_{WFn}$.

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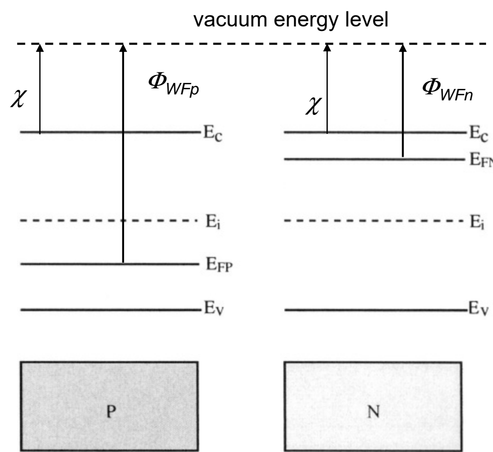
J.-P. Colinge, C.A. Colinge, "Physics of Semiconductor Devices", Springer 2002



(Electron affinity χ is equal for *n*- and *p*-type semiconductor samples.

$$E_{Fn} - E_i \approx k_B T \cdot \ln\left(\frac{N_D}{n_i}\right) \qquad E_i - E_{Fp} \approx k_B T \cdot \ln\left(\frac{N_A}{n_i}\right)$$

here E_i is a Fermi level for intrinsic semiconductor.

Creation of *pn* junction results in diffusion of electrons from *n*–type part to *p*–type part and diffusion of holes from *p*–type part to *n*–type part.

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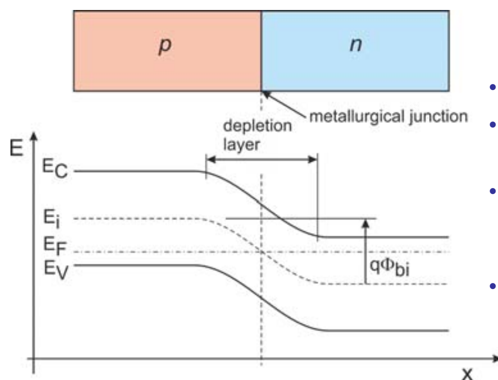

- Shorted juction – zero bias voltage.
- Average electron energies are equalized at entire semiconductor sample.
- Therefore, for *n*-type part, conduction and valence bands shifted downwards on energy axis with respect to *p*-type part.
- Built-in potential difference Φ_{bi} appears.

$$\Phi_{bi} = \frac{(E_{Fn} - E_i) + (E_i - E_{Fp})}{q} \approx \frac{k_B T}{q} \cdot \ln\left(\frac{N_D}{n_i}\right) + \frac{k_B T}{q} \cdot \ln\left(\frac{N_A}{n_i}\right)$$

$$\Phi_{bi} \approx \frac{k_B T}{q} \cdot \ln\left(\frac{N_D N_A}{n_i^2}\right) \qquad \text{gdzie} \qquad V_T = \frac{k_B T}{q}$$

T = 300 K, $V_T \approx 25$ mV at room temperature

Electron and hole currents are zero at equilibrium

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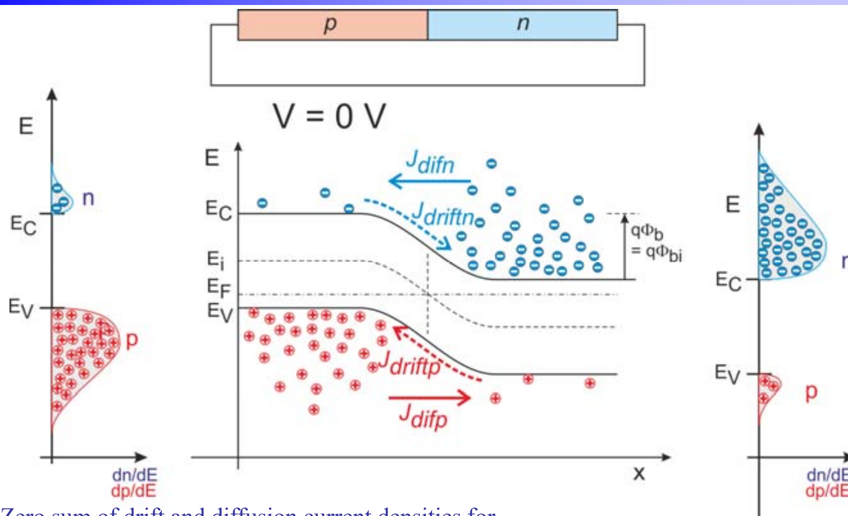

Zero sum of drift and diffusion current densities for electrons, as well as for holes:

$$J_n = J_{driftn} + J_{difn} = 0$$

$$J_p = J_{driftp} + J_{difp} = 0$$

Note: arrows show directions of fluxes, not of currents.

Positive bias of *p*–type region with respect to *n*–type region – in forward direction – results in decreased potential barrier Φ_b of *pn* junction

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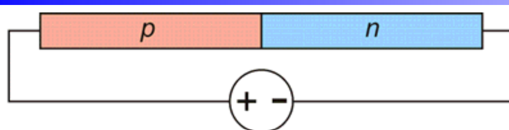
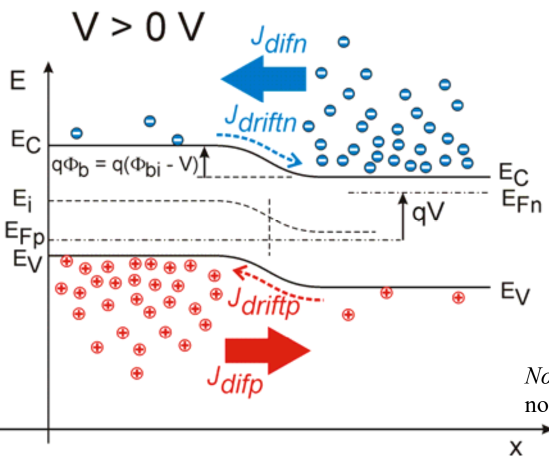




Effects of decreased potential barrier Φ_b:

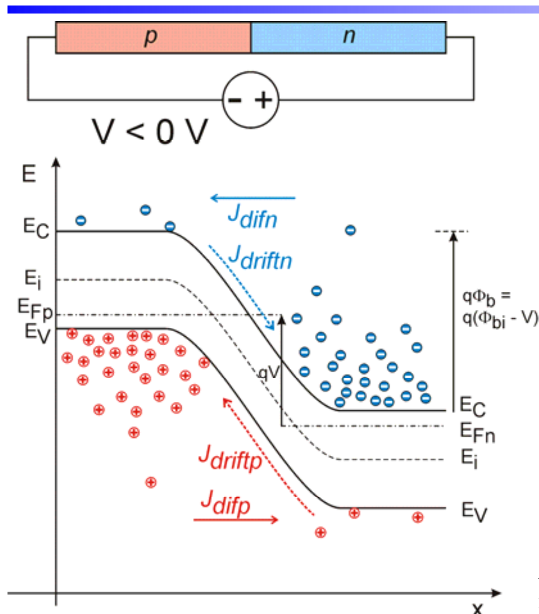
- increased densities of diffusion currents for electrons J_{difn} and for holes J_{difp};
- decreased densities of drift currents for electrons J_{driftn} and for holes J_{driftp}.

Diffusion currents dominate.

In result, a large forward current flows in the diode, and its direction is as for J_{difp}, that is from the *p*-type region to the *n*-type region.

Note: arrows show directions of fluxes, not of currents.

Reverse bias of *p*–type region with respect to *n*–type region – in reverse direction – results in increased potential barrier Φ_b of *pn* junction



Effects of increased potential barrier Φ_b:

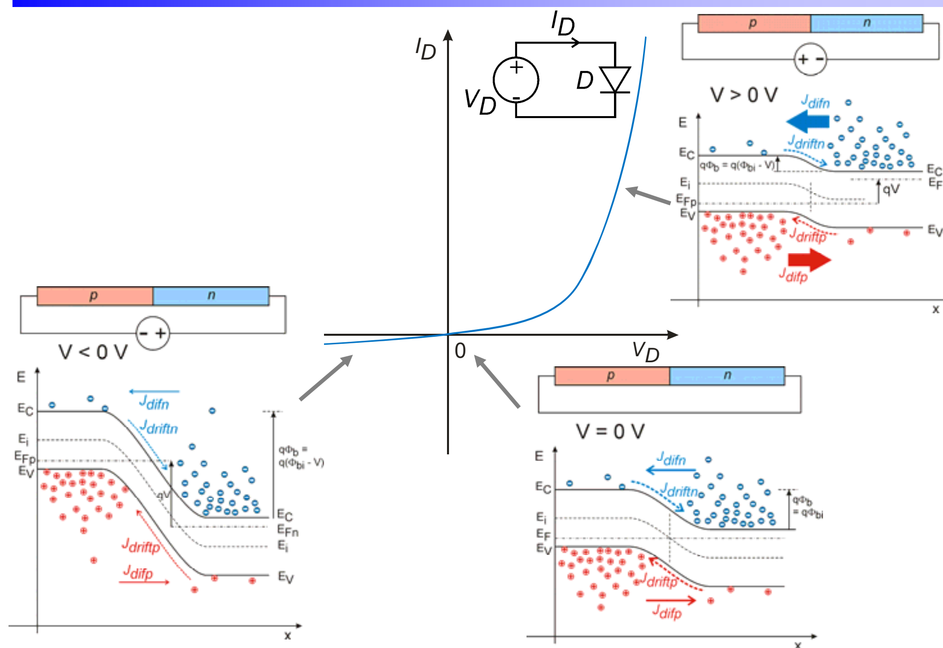
- substantially reduced densities of diffusion currents for electrons J_{difn} and for holes J_{difp};
- decreased densities of drift currents for electrons J_{driftn} and for holes J_{driftp}.

Drift currents dominate. They are very small, because the hole concentration is very small in *n*-type region, and the electron concentration is very small in *p*-type region.

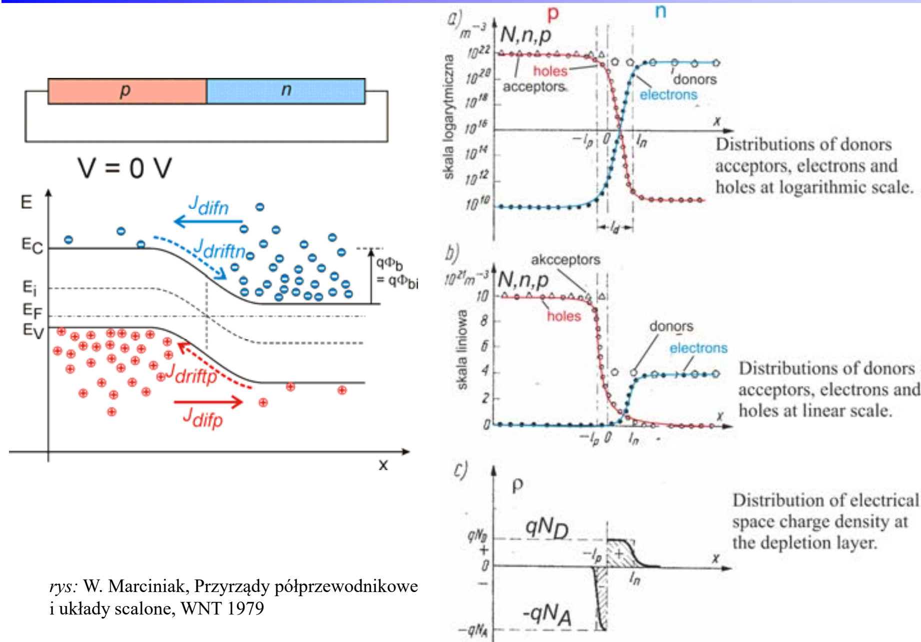
A very small reverse current flows in the diode, and its direction is as for J_{driftp}, that is from the *n*-type region to the *p*-type region.

Note: arrows show directions of fluxes, not of currents.

Current-voltage characteristics of *pn* junction (qualitatively)



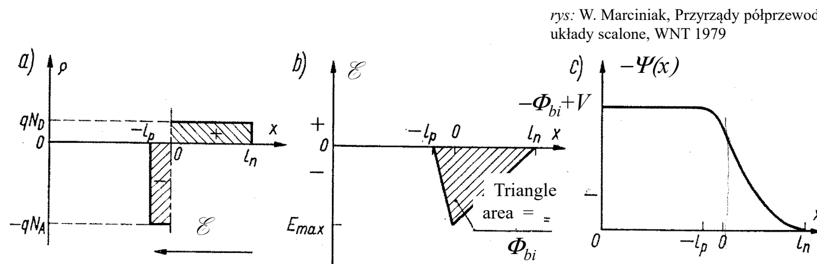
Distributions of electrons and holes in depletion layer of *pn* junction - qualitatively



rys: W. Marciniak, Przyrządy półprzewodnikowe i układy scalone, WNT 1979

Capacitance related to depletion layer of *pn* junction - junction capacitance (barrier capacitance)

rys: W. Marciniak, Przyrządy półprzewodnikowe i układy scalone, WNT 1979



Depletion layer width l_d depends on the voltage biasing the junction

$$l_d = \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{q} \cdot \frac{N_D + N_A}{N_D N_A} \cdot (\Phi_{bi} - V)}$$

- The change in the depletion layer width l_d is related to the changing non-compensated electrical charge of ionized donors on the *n*-type side, as well as changing charge of ionized acceptors on *p*-type side. The absolute values of the both charges are equal.
- We have, therefore, a junction capacitance per area [F/m^2] of:

$$C_j / A_D \approx \frac{\varepsilon_{Si}\varepsilon_0}{l_d} \qquad C_j / A_D \approx \frac{\varepsilon_{Si}\varepsilon_0}{\sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{q} \cdot \frac{N_D + N_A}{N_D N_A} \cdot (\Phi_{bi} - V)}}$$

here A_D is an area of the junction.

Junction capacitance can be used as a capacitance of a value tuned with the DC bias, most conveniently at reverse DC bias

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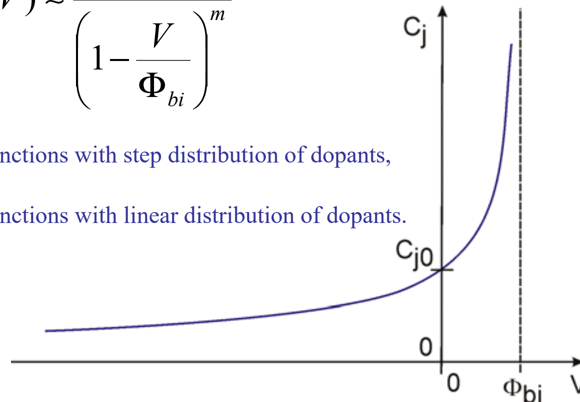
$$C_j(V) \approx \frac{C_{j0}}{\left(1 - \frac{V}{\Phi_{bi}}\right)^m}$$

$m = 1/2$ - for junctions with step distribution of dopants,

$m = 1/3$ - for junctions with linear distribution of dopants.



Diodes predestinated for applications as voltage-tuned capacitors are refered to as capacitance diodes or varactors.

Capacitance related to charges of excess concentrations of electrons and holes in quasi-neutral regions – diffusion capacitance

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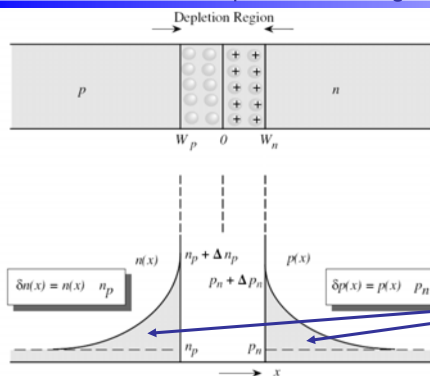
U.Mishra, J.Singh, Semiconductor Device Physics and Design, Springer 2007

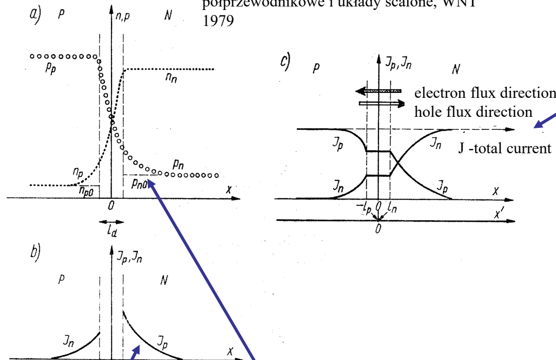


Excess charges of minority carriers stored in quasi-neutral regions for forward bias.

- At a forward bias of a junction, the diffusion of electrical charge carriers leads to injection of holes from the p-type side to the n-type side, where they are minority carriers. The electron concentration increases there also to keep the electrical neutrality.
- And electrons are injected from the n-type region to p-type region, which is accompanied with increase in hole concentration to keep the electrical neutrality.
- Total charges of injected carriers depend exponentially on the value of applied bias voltage.
- The dependence of the total charges of injected minority carriers stored in the forward biased junction indicates existence of an additional capacitance – a diffusion capacitance.

Voltage dependence of forward current of *pn* junction

Forward bias of a junction, $V > 0$ V.



We obtain – exponentially decaying excess minority electrons and holes distributions, as functions of x.

and, accordingly, exponentially decaying distributions of electron and hole current densities.

Total current density J remains constant:

$$J = J_n + J_p$$

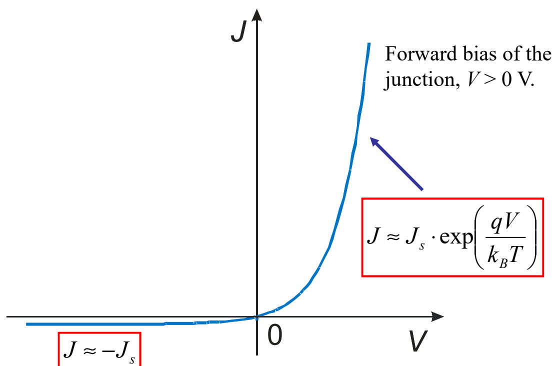
$$J \approx J_s \cdot \left[\exp\left(\frac{qV}{k_B T} \right) - 1 \right]$$

Here, the saturation current density J_s in a simple case of a step junction is expressed as:

$$J_s \approx q n_i^2 \left(\frac{1}{N_A} \sqrt{\frac{D_n}{\tau}} + \frac{1}{N_D} \sqrt{\frac{D_p}{\tau}} \right)$$

Voltage dependence of *pn* junction current

Recombination of exceess holes and electrons injected into the quasi-neutral regions at the forward bias of the junction makes that fresh carriers are being injected continuously. The current value remains constant for the constant bias voltage.



$$J \approx J_s \cdot \exp\left(\frac{qV}{k_B T} \right)$$

$$J \approx -J_s$$

Reverse bias of the junction, $V > 0$ V.

Total current density J remains constant:

$$J = J_n + J_p$$

$$J \approx J_s \cdot \left[\exp\left(\frac{qV}{k_B T} \right) - 1 \right]$$

Here, the saturation current density J_s in a simple case of a step junction is expressed as:

$$J_s \approx q n_i^2 \left(\frac{1}{N_A} \sqrt{\frac{D_n}{\tau}} + \frac{1}{N_D} \sqrt{\frac{D_p}{\tau}} \right)$$

Current-voltage characteristic of ideal *pn* junction

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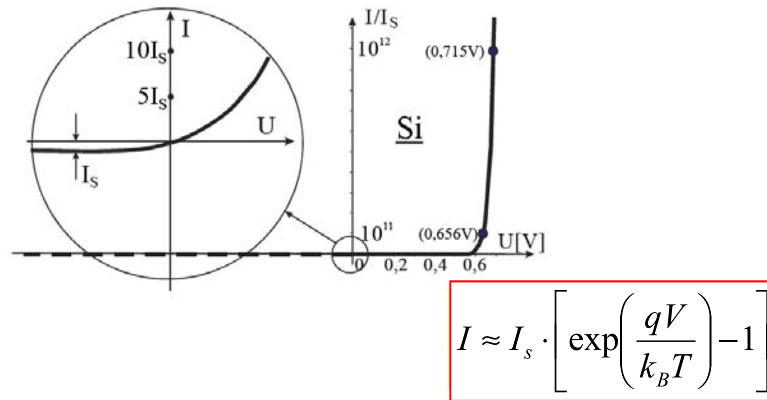

$$I \approx I_s \cdot \left[\exp\left(\frac{qV}{k_B T} \right) - 1 \right]$$

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IV draft

Current-voltage characteristic of real *pn* diode

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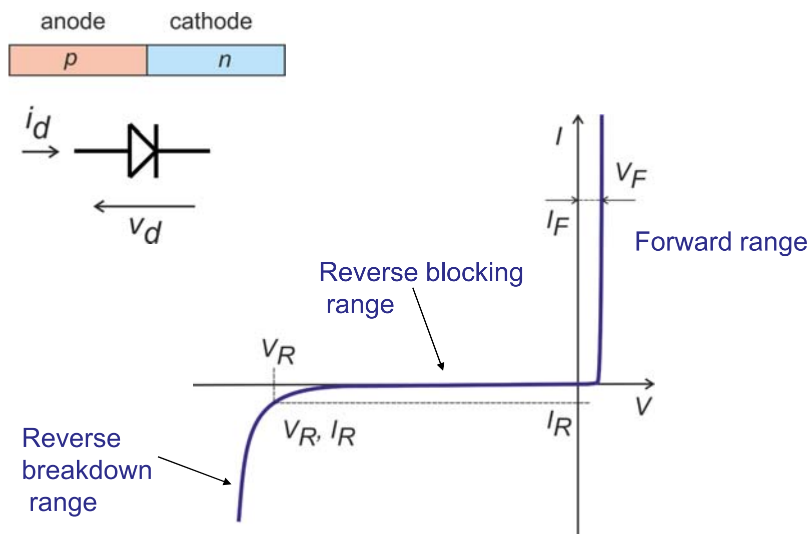
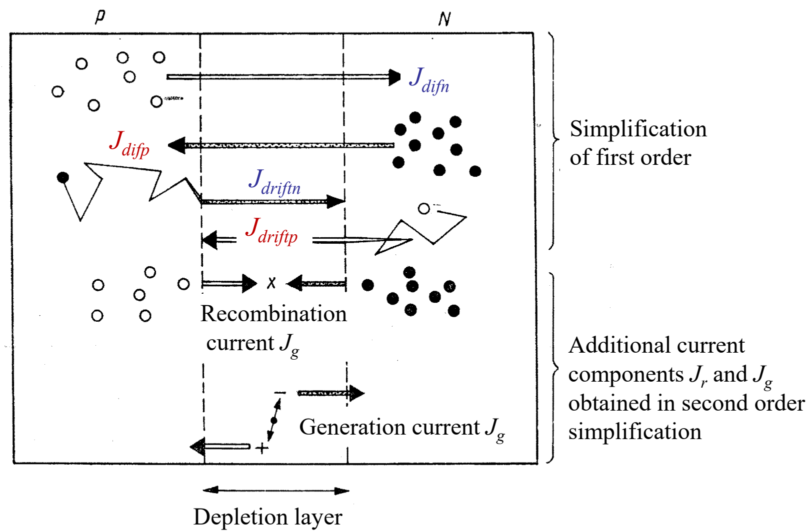


More realistic characteristics may be obtained if additional effects are taken into account



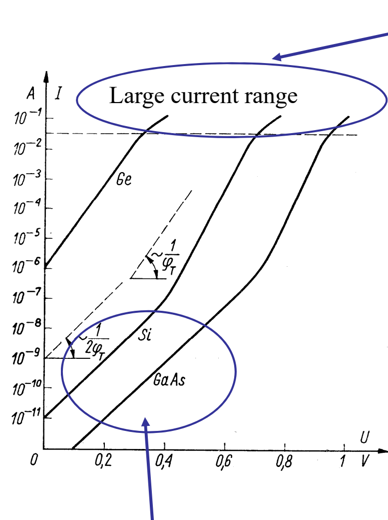
Simplification of first order

Additional current components J_r and J_g obtained in second order simplification

from: W. Marciniak, Przyrządy półprzewodnikowe i układy scalone, WNT 1979

Characteristics of real diodes at forward bias

Series resistances r_s should be taken into account for large currents . In addition, concentration of minority and majority carriers can be nearly equal, $n \approx p$.



Electron-hole recombination in the depletion layer affects characteristics at small currents.

Approximate expression for current-voltage characteristics of a real diode at forward bias ($V > 0$)

$$I_{Ddc} \approx I_s \cdot \left\{ \exp\left[\frac{q(V_{Ddc} - I_{Ddc} r_s)}{n_{ideal} k_B T} \right] - 1 \right\}$$

$$\downarrow$$

$$I_{Ddc} \approx I_s \cdot \exp\left(\frac{q V_{Ddc}}{n_{ideal} k_B T} \right)$$

from: W. Marciniak, Przyrządy półprzewodnikowe i układy scalone, WNT 1979

Reverse currents of *pn* diodes for reverse blocking range

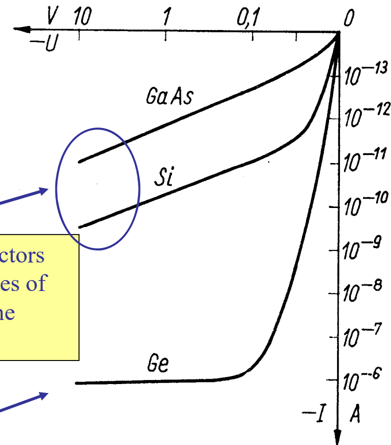
For „ideal" *pn* junction at reverse bias for reverse blocking range

$$J \approx J_s \cdot \left[\exp\left(\frac{qV}{k_B T}\right) - 1\right]$$

$$\downarrow$$

$$I \approx -I_s$$

For Si diodes and diodes made of semiconductors having larger bandgaps E_g usually the densities of generation currents J_g are much larger than the densities of saturation currents J_s .

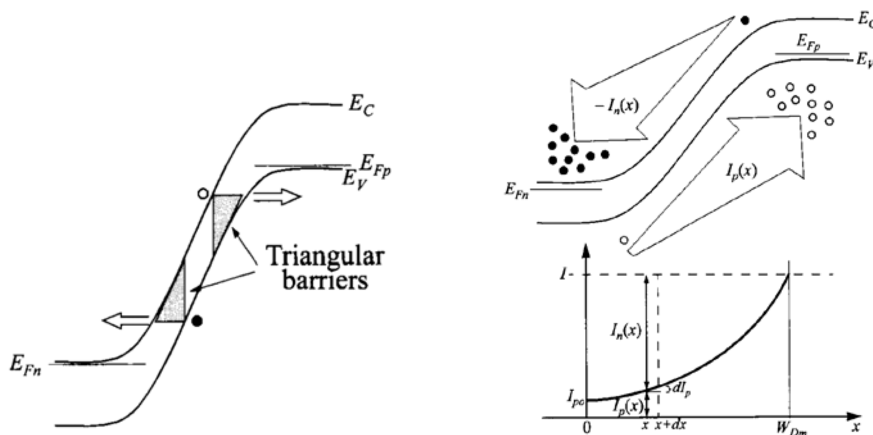


Saturation current J_s usually dominates for germanium diodes, because of small E_g for Ge.

from: W. Marciniak, Przyrządy półprzewodnikowe i układy scalone, WNT 1979

Reverse currents of *pn* diodes at breakdown range

Energy band diagrams showing breakdown mechanisms.



Tunneling mechanism (Zener mechanism)

Avalanche multiplication (example initiated by hole current I_{p0}).

S.M. Sze, K.K. Ng, "Physics of Semiconductor Devices", 3 ed., Wiley 2007, p. 104

Effect of temperature on current of *pn* junction

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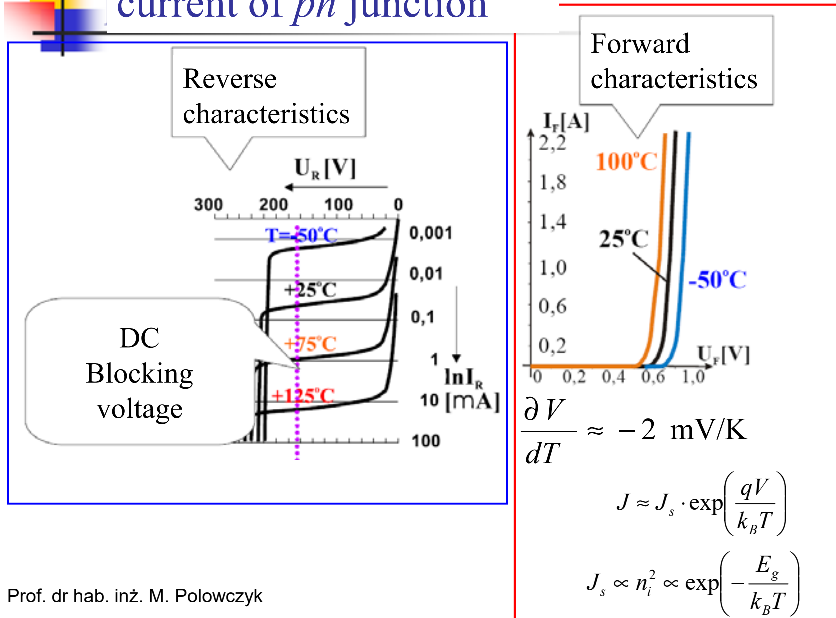

$$\frac{\partial V}{dT} \approx -2 \text{ mV/K}$$

$$J \approx J_s \cdot \exp\left(\frac{qV}{k_B T}\right)$$

$$J_s \propto n_i^2 \propto \exp\left(-\frac{E_g}{k_B T}\right)$$

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Effect of temperature on current of *pn* junction

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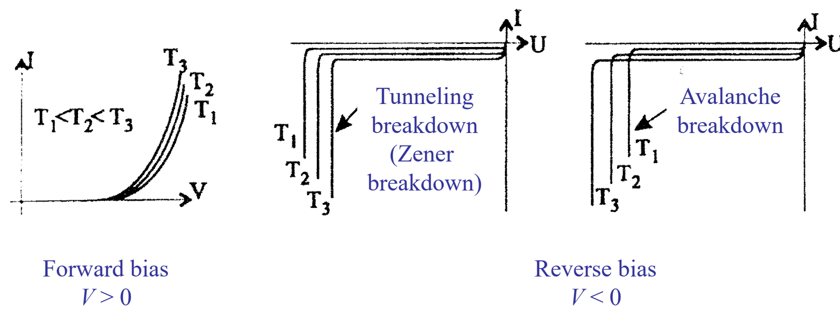
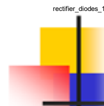


Forward bias
$V > 0$

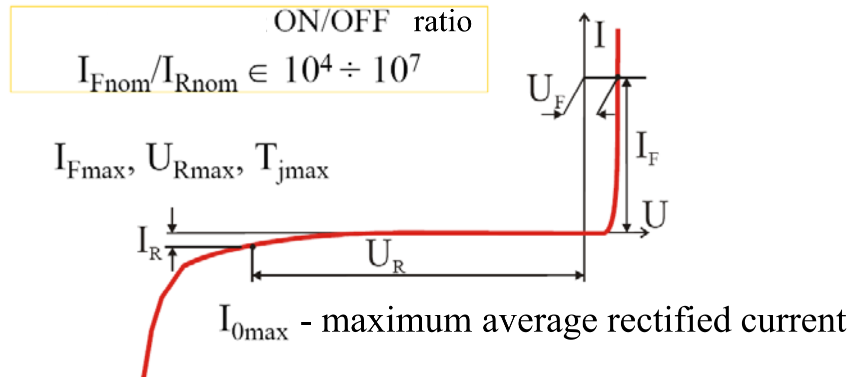
Reverse bias
$V < 0$

M.Polowczyk, E.Klugmann, Przyrządy Półprzewodnikowe", Wyd.PG, 2001



Diodes for rectifiers

A property that makes diodes useful for converting the AC current into direct current that is for rectifying is nonlinearity of its current-voltage characteristic.



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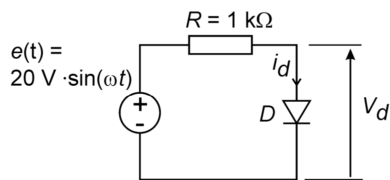
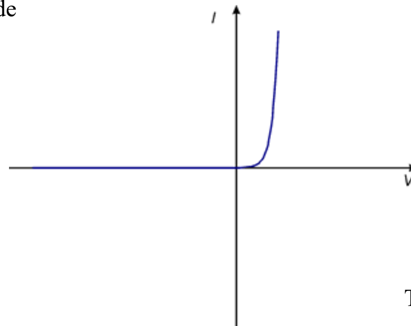
Diode in a rectifier circuit – large signal operation

Silicon diode having the breakdown voltage larger than 20 V and known *I-V* characteristic was applied in the rectifier circuit. Determine time dependencies of the diode current $i_d(t)$ and the diode voltage $v_d(t)$. (For low frequencies, when diode capacitances may be neglected.)



Current-voltage static characteristic of the diode



Loop equation

$$e = i_d(t) \cdot R + v_d(t)$$

that is

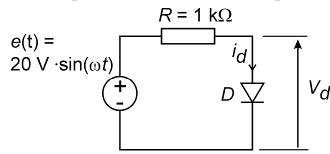
$$i_d = \frac{e(t) - v_d(t)}{R}$$

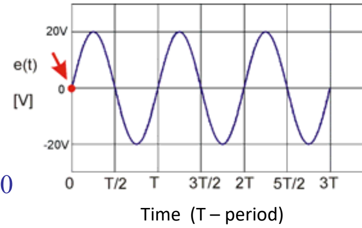
valid at any time instant.

This equation represents the load line.

Diode in a rectifier circuit – large signal operation

Silicon diode having the breakdown voltage larger than 20 V and known *I*-*V* characteristic was applied in the rectifier circuit. Determine time dependencies of the diode current $i_d(t)$ and the diode voltage $v_d(t)$. (For low frequencies, when diode capacitances may be neglected.)





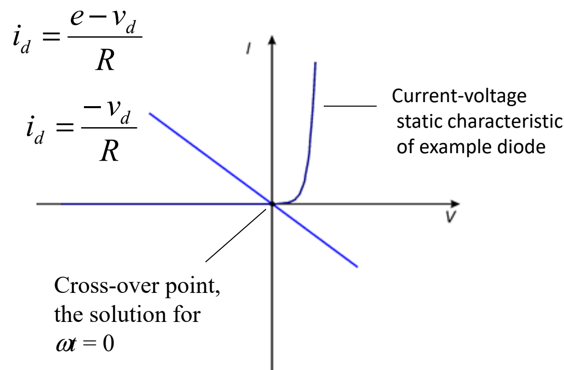
for $\omega t = 0$

$e(t) = 20\text{ V}\sin(\omega t) = 0$

Load line:

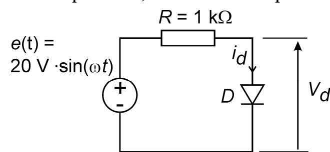
$$i_d = \frac{e - v_d}{R}$$

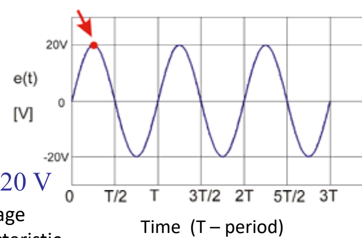
$$i_d = \frac{-v_d}{R}$$



Diode in a rectifier circuit – large signal operation

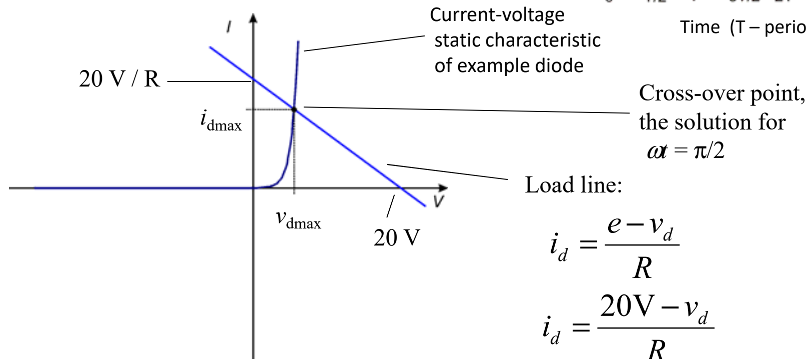
Silicon diode having the breakdown voltage larger than 20 V and known *I*-*V* characteristic was applied in the rectifier circuit. Determine time dependencies of the diode current $i_d(t)$ and the diode voltage $v_d(t)$. (For low frequencies, when diode capacitances may be neglected.)





for $\omega t = \pi/2$

$e(t) = 20\text{ V}\sin(\omega t) = 20\text{ V}$



$$i_d = \frac{e - v_d}{R}$$

$$i_d = \frac{20\text{V} - v_d}{R}$$

Diode in a rectifier circuit – large signal operation

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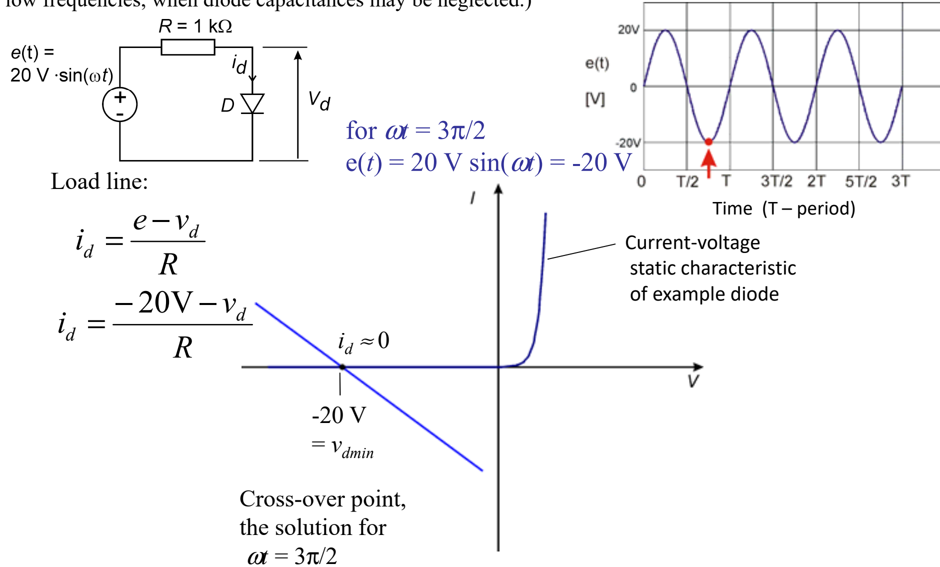
Silicon diode having the breakdown voltage larger than 20 V and known *I-V* characteristic was applied in the rectifier circuit. Determine time dependencies of the diode current $i_d(t)$ and the diode voltage $v_d(t)$. (For low frequencies, when diode capacitances may be neglected.)



Diode in a rectifier circuit – large signal operation

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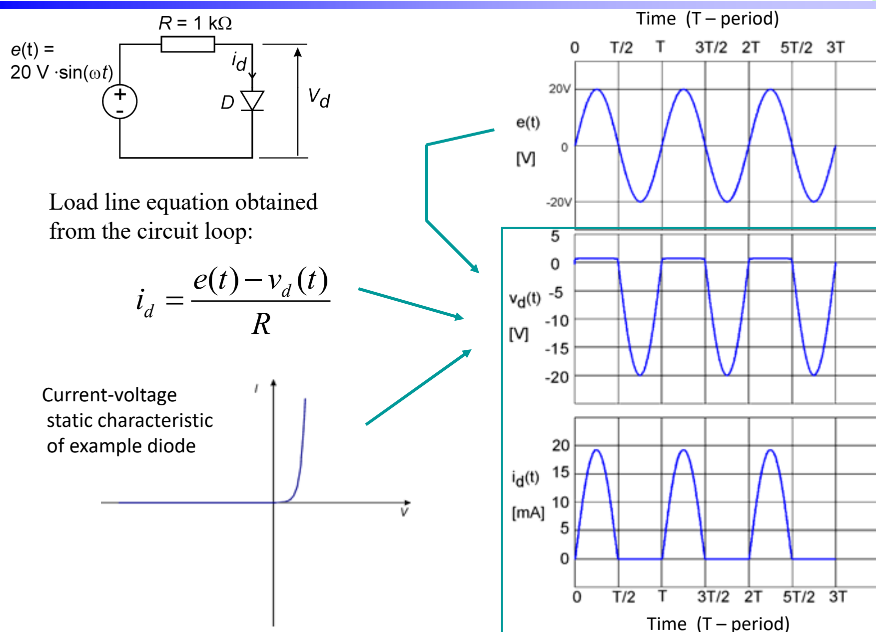
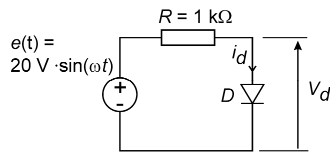
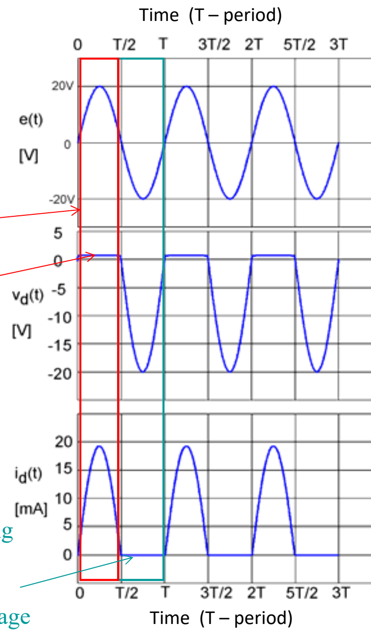


Diode in a rectifier circuit – large signal operation





Forward biased diode

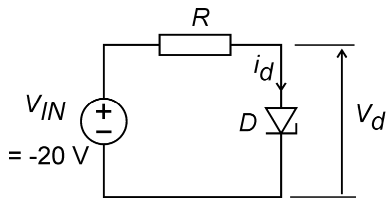
Forward voltage of Si diode is approx. 0,7 V

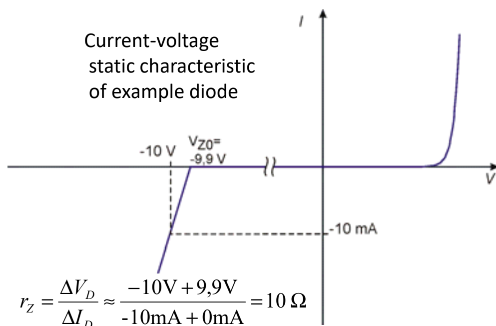
Current-voltage static characteristic of example diode

Reverse biase diode (in a blocking direction). The diode current is small as long as the voltage is smaller than the breakdown voltage

Stabilization diode ("Zener" diode) in voltage stabilizer circuit

Silicon stabilization diode of known current-voltage characteristics was applied in a circuit as below. Determine the diode current I_D and the diode voltage V_D.





$$r_Z = \frac{\Delta V_D}{\Delta I_D} \approx \frac{-10\text{V} + 9{,}9\text{V}}{-10\text{mA} + 0\text{mA}} = 10\,\Omega$$

Loop equation:

$$V_{IN} = I_D \cdot R + V_D$$

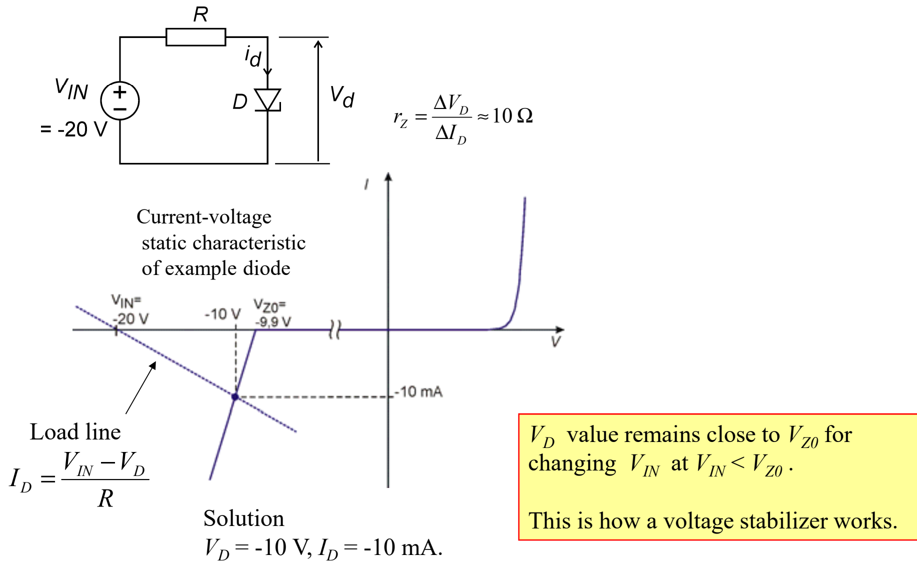
that is

$$I_D = \frac{V_{IN} - V_D}{R}$$

This equation represents the load line.

Stabilization diode ("Zener" diode) in voltage stabilizer circuit

Silicon stabilization diode of known current-voltage characteristics was applied in a circuit as below. Determine the diode current I_D and the diode voltage V_D.



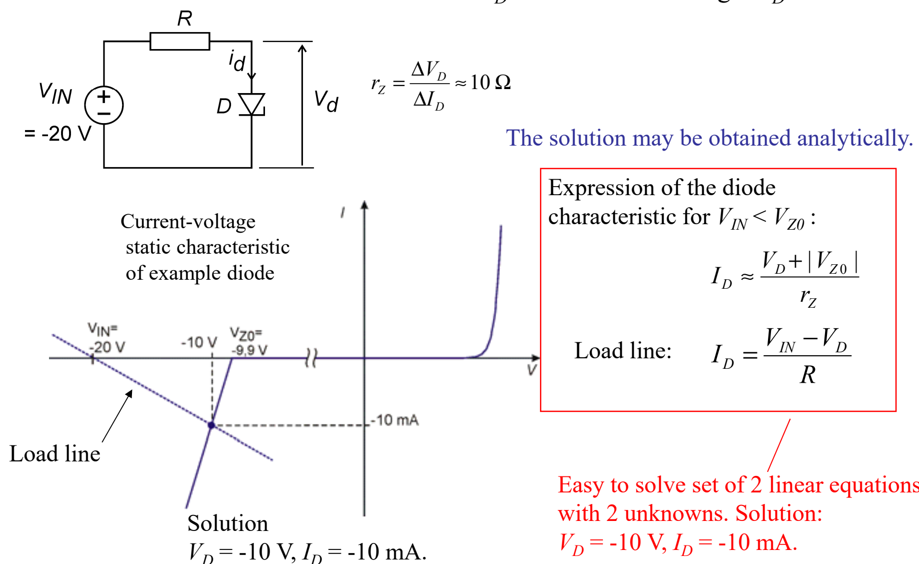
Solution
V_D = -10 V, I_D = -10 mA.

V_D value remains close to V_{Z0} for changing V_{IN} at $V_{IN} < V_{Z0}$.

This is how a voltage stabilizer works.

Stabilization diode ("Zener" diode) in voltage stabilizer circuit

Silicon stabilization diode of known current-voltage characteristics was applied in a circuit as below. Determine the diode current I_D and the diode voltage V_D.



The solution may be obtained analytically.

Expression of the diode characteristic for $V_{IN} < V_{Z0}$:

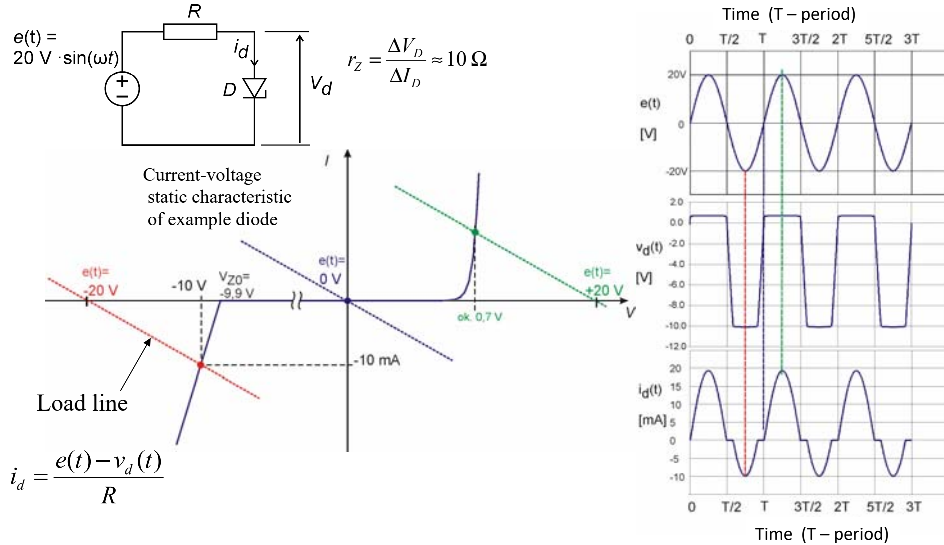
$$I_D \approx \frac{V_D + |V_{Z0}|}{r_Z}$$

Load line: $$I_D = \frac{V_{IN} - V_D}{R}$$

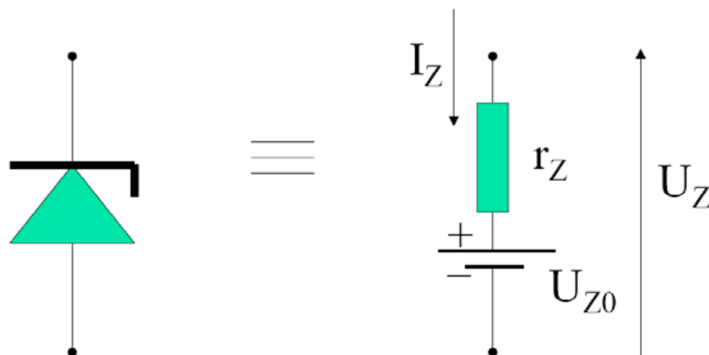
Solution
V_D = -10 V, I_D = -10 mA.

Easy to solve set of 2 linear equations with 2 unknowns. Solution:
V_D = -10 V, I_D = -10 mA.

Silicon stabilization diode of known current-voltage characteristics was applied in a circuit as below. The magnitude of the AC voltage source *e(t)* is larger than the stabilization voltage of the diode – i.e. the breakdown voltage. Determine time dependencies of the diode current $i_d(t)$ and the diode voltage $v_d(t)$.



Equivalent electrical circuit of a diode operating in the stabilization range



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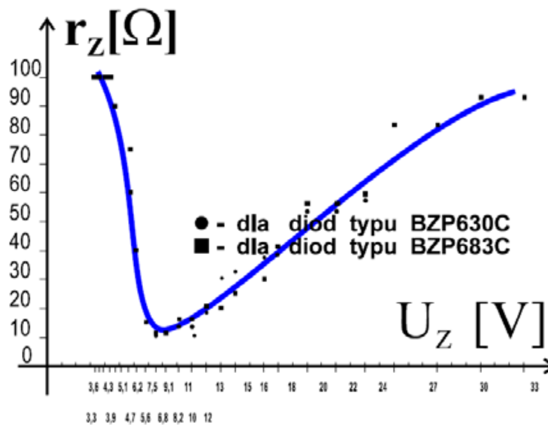
Differential resistance of stabilization diodes



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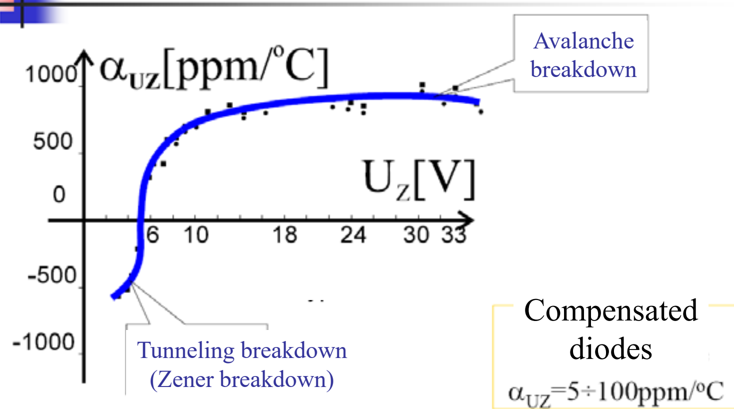
Temperature coefficient of stabilization voltage



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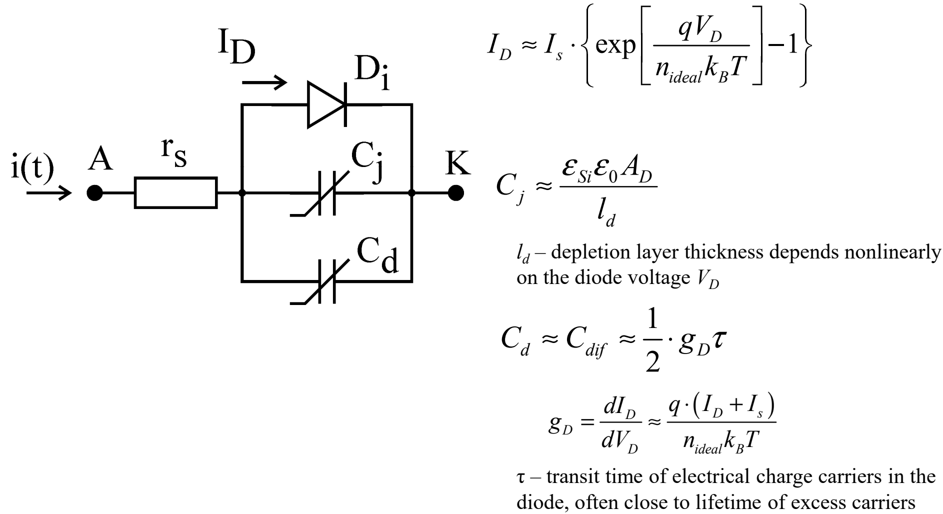
Large signal dynamic operation of a diode – pulse operation

Nonlinear equivalent diode circuits should be used at large magnitudes of time-dependent, fat-changing signals.



$$I_D \approx I_s \cdot \left\{ \exp\left[\frac{qV_D}{n_{ideal} k_B T} \right] - 1 \right\}$$

$$C_j \approx \frac{\varepsilon_{Si}\varepsilon_0 A_D}{l_d}$$

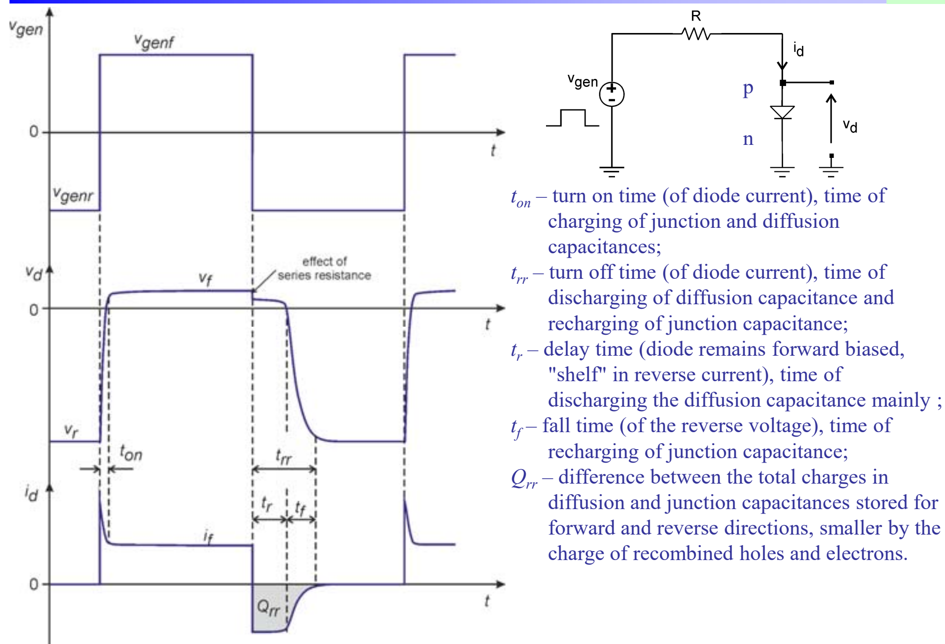
l_d – depletion layer thickness depends nonlinearly on the diode voltage V_D

$$C_d \approx C_{dif} \approx \frac{1}{2} \cdot g_D \tau$$

$$g_D = \frac{dI_D}{dV_D} \approx \frac{q \cdot (I_D + I_s)}{n_{ideal} k_B T}$$

τ – transit time of electrical charge carriers in the diode, often close to lifetime of excess carriers

Pulse operation of a diode



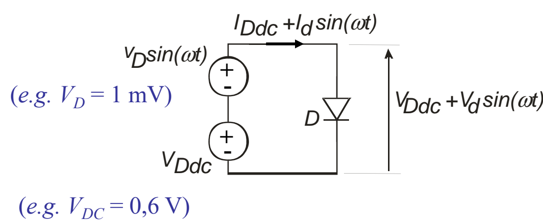
t_{on} – turn on time (of diode current), time of charging of junction and diffusion capacitances;

t_{rr} – turn off time (of diode current), time of discharging of diffusion capacitance and recharging of junction capacitance;

t_r – delay time (diode remains forward biased, "shelf" in reverse current), time of discharging the diffusion capacitance mainly ;

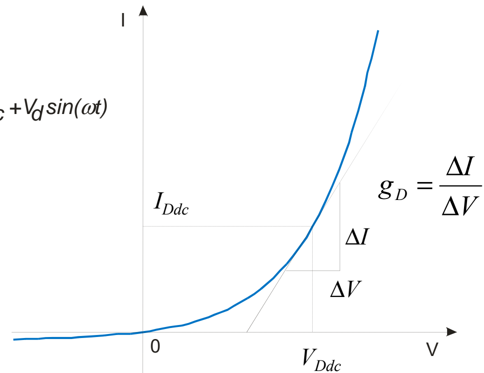
t_f – fall time (of the reverse voltage), time of recharging of junction capacitance;

Q_{rr} – difference between the total charges in diffusion and junction capacitances stored for forward and reverse directions, smaller by the charge of recombined holes and electrons.



(e.g. $V_D = 1$ mV)

(e.g. $V_{DC} = 0{,}6$ V)



The best method is to solve the electron and hole transport equations linearized around the operation point of V_{Ddc} , I_{Ddc} .

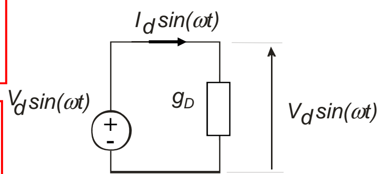
Usually a simpler method is used, which is linearization of the diode characteristic around the operation point of V_{Ddc} , I_{Ddc} .

For signals of low frequencies:

$$g_D = \frac{I_{Ddc} + I_s}{n_{ideal} V_T}$$

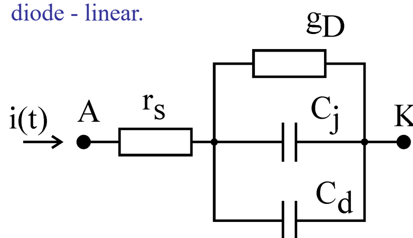
At forward bias:

$$g_D \approx \frac{I_{Ddc}}{n_{ideal} V_T}$$



Series resistance r_S should be taken into account.
For high frequencies the junction capacitance C_j and the diffusion capacitance C_{dif} should be included in the equivalent circuit.

Small signal equivalent circuit of *pn* diode - linear.



$$g_D = \frac{I_{Ddc} + I_s}{n_{ideal} V_T}$$

$$C_j \approx \frac{\varepsilon_{Si} \varepsilon_0 A_D}{l_d}$$

Note: All elements are linear. The values of g_D, C_j and C_d should be taken as for the diode biased at (V_{DC}, I_{DC}).

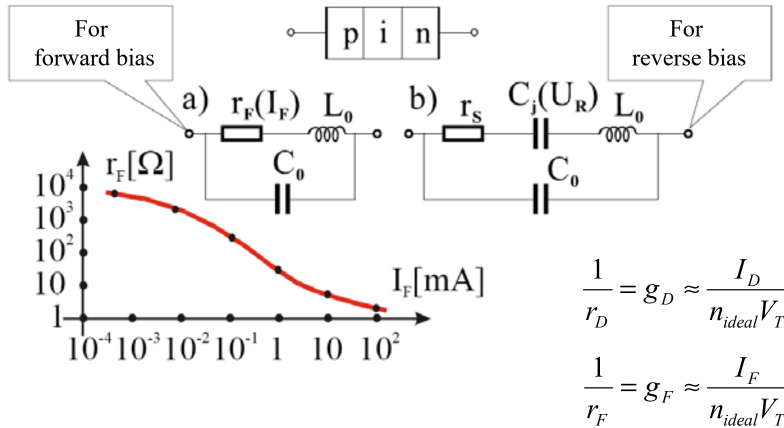
$C_d \approx C_{dif}$ – mainly a diffusion capacitance. Represents the charge of electrons and holes stored at the diode. Significant only at forward bias.

$$C_d \approx \frac{1}{2} \cdot g_D \tau$$

Here τ is a transit time of electrical charge carriers in the diode. At the simplest case $\tau = \tau_n = \tau_p$ - lifetime of excess carriers

Microwave diodes

Mixer, attenuator and switching diodes



$$\frac{1}{r_D} = g_D \approx \frac{I_D}{n_{ideal} V_T}$$

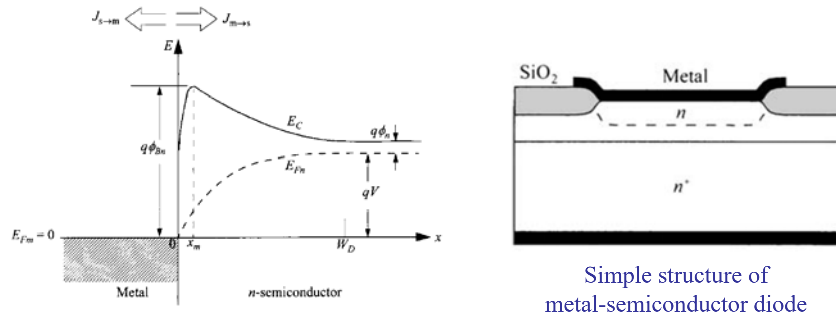
$$\frac{1}{r_F} = g_F \approx \frac{I_F}{n_{ideal} V_T}$$

Rys: Prof. dr hab. inż. M. Polowczyk

Metal-semiconductor diode - Schottky diode

Metal-semiconductor diode - Schottky diode

- Semiconductors and metals may have different values of workfunctions.
- Therefore, it is possible to make a diode with a potential barrier at a metal-semiconductor interface.
- There is no injection and storing of minority electrical carriers in this device. A diode of this kind is very "fast".
- The high frequency operation and switching time are limited by a transit time of carriers, a junction capacitance and a series resistance.



Simple structure of metal-semiconductor diode

Fig. 17 Energy-band diagram incorporating the Schottky effect to show the derivations of thermionic-emission-diffusion theory and tunneling current.

Diode of metal – silicon of n–type. Energy band diagram.

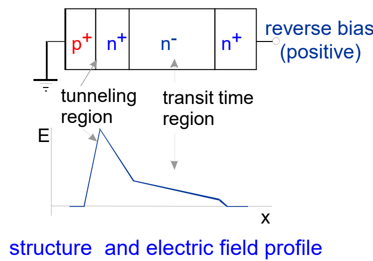
S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006

Millimeter Wave and Terahertz Wave Oscillators with TUNNETT Diodes

TUNNETT_tytul

TUNNETT - transit time oscillator diode with tunneling injection of electrons

Transit time of electrons in a diode in combination with impact ionization breakdown or with tunneling breakdown at special conditions may result in oscillations. It is used for designing of IMPATT and TUNNETT microwave oscillators.



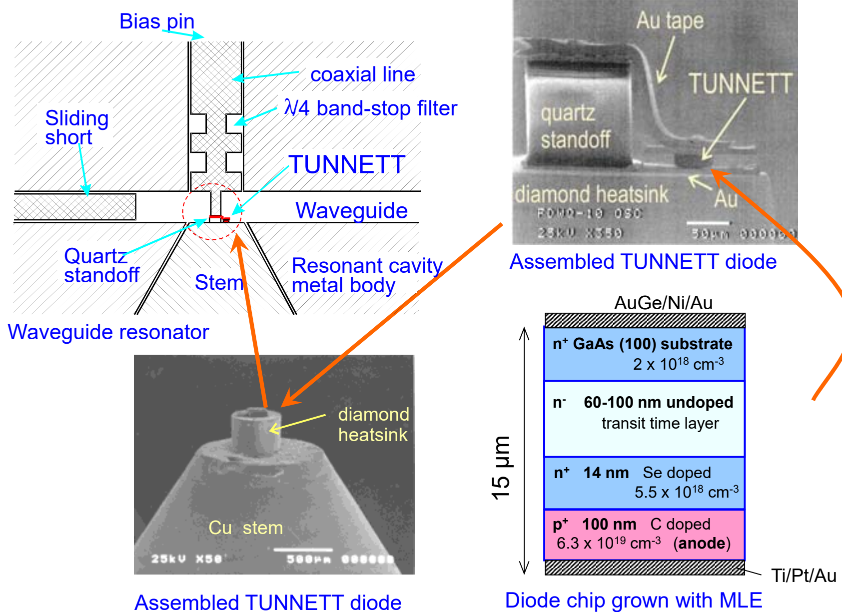
structure and electric field profile

TUNNETT invention:
Nishizawa 1958

first operation:
Nishizawa 1968

TUNNETT_intro

TUNNETT oscillator with waveguide resonant cavity



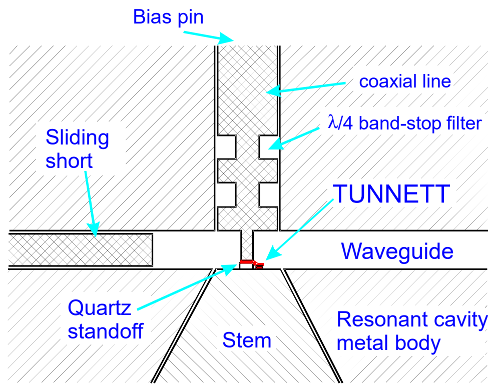
Assembled TUNNETT diode

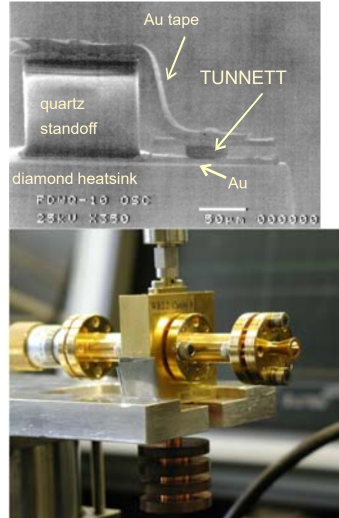
Assembled TUNNETT diode

Diode chip grown with MLE

waveguide resonant cavities

WR-2.2: 0.559 × 0.279 mm for band of f_{cutoff} = 268 GHz to 500 GHz
WR-1.5: 0.381 × 0.191 mm for band of f_{cutoff} = 393 GHz to 750 GHz
WR-1.2: 0.305 × 0.152 mm for band of f_{cutoff} = 492 GHz to 900 GHz
WR-1.0: 0.254 × 0.127 mm for band of f_{cutoff} = 590 GHz to 1100 GHz





cavities - flat

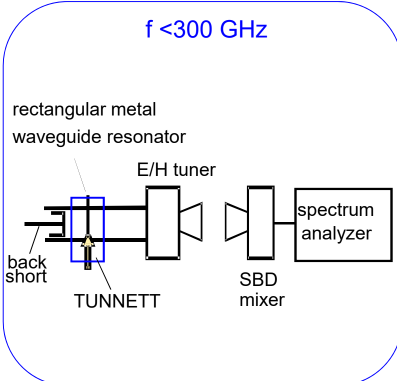
TUNNETT oscillators with waveguide resonant cavities

waveguide resonators and measurement configurations

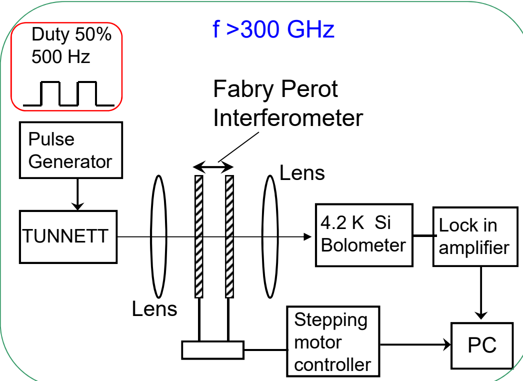
WR-3 : 0.864 × 0.432 mm for band of f_{cutoff} = 174 GHz to 325 GHz
WR-2.2: 0.559 × 0.279 mm for band of f_{cutoff} = 268 GHz to 500 GHz
WR-1.5: 0.381 × 0.191 mm for band of f_{cutoff} = 393 GHz to 750 GHz
WR-1.2: 0.305 × 0.152 mm for band of f_{cutoff} = 492 GHz to 900 GHz
WR-1.0: 0.254 × 0.127 mm for band of f_{cutoff} = 590 GHz to 1100 GHz

High frequency

f <300 GHz

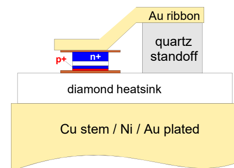


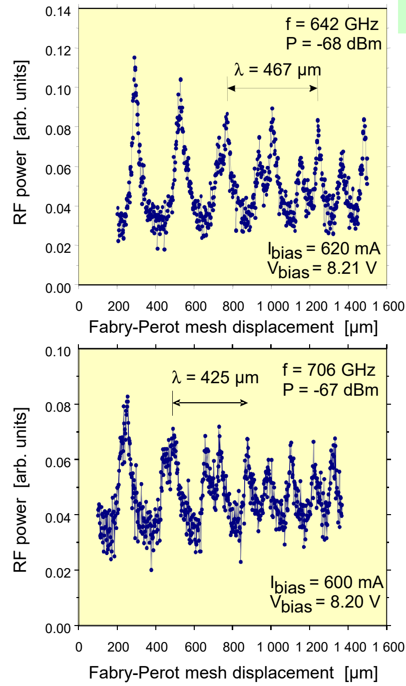
f >300 GHz



600 - 706 GHz CW, fundamental mode TUNNETT oscillation in metal, rectangular WR-1.0 type cavity (0.254 × 0.127 mm)

p^{++} C doped 100 nm 6.3e19 cm^{-3} anode
n^{+} Se doped 14 nm 5.5e18 cm^{-3}
undoped 75 nm transit time layer
n^{+} S.I. (100) GaAs 2e18 cm^{-3} substrate





600-706GHz WR 1.0 spectra 131xls

Bipolar transistors

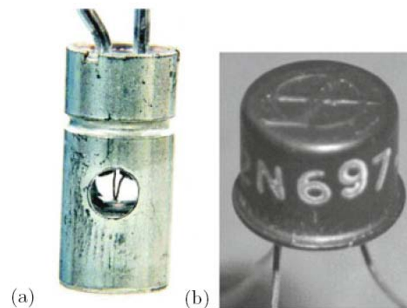
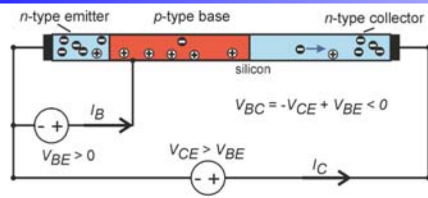


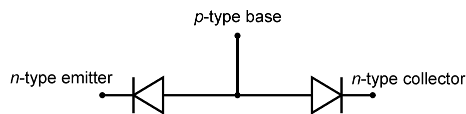
Fig. 23.2. (**a**) First commercial, developmental (point contact) transistor from BTL (Bell Telephone Laboratories) with access holes for adjustment of the whiskers pressing on a piece of Ge, diameter 7/32"=5 mm, 1948. (**b**) First high-performance silicon transistor (npn mesa technology), model 2N697 from Fairchild Semiconductor, 1958 (at \$200, in 1960 \$28.50). The product number is still in use (now \$0.95)

M. Grundmann, The Physics of Semiconductors ..., Springer 2010

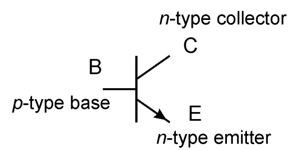
npn bipolar transistor



Semiconductor structure of *npn* transistor

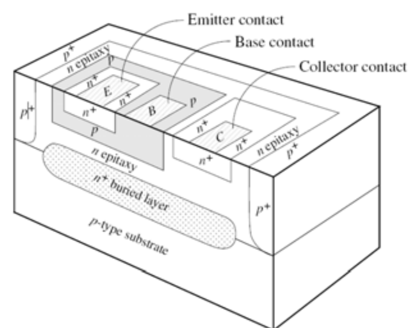


Anode-to-anode series connection of two *pn* diodes

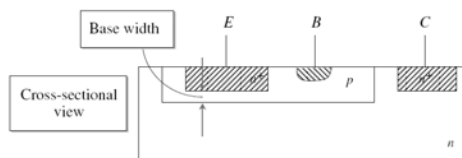


Circuit symbol of *npn* transistor

Bipolar *npn* transistor in silicon integrated circuit

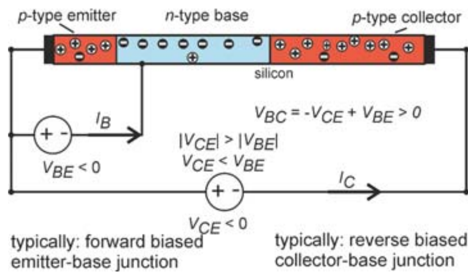


epitaxy – growing a monocrystal on a monocrystal substrate.

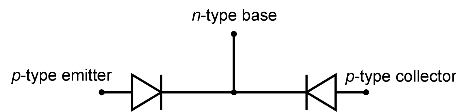


rys: U.Mishra, J.Singh "Semiconductor Device Physics and Design", Springer 2007

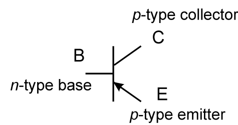
pnp bipolar transistor



Semiconductor structure of *pnp* transistor



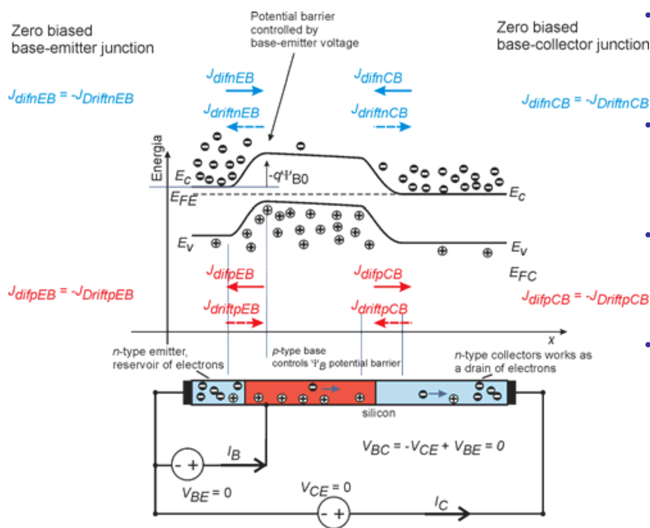
Cathode-to-cathode series connection of two *pn* diodes



Circuit symbol of *pnp* transistor

Band diagram of a bipolar trasistor in thermal equilibrium, at $V_{BE} = 0$ and $V_{BC} = 0$

Note: arrows show directions of fluxes, not of currents.



- The diffusion and drift electron current components compensate each other at the base-emitter junction.
- Also the diffusion and drift hole current components compensate each other at the base-emitter junction.
- The diffusion and drift electron current components compensate each other at the base-collector junction as well.
- Also the diffusion and drift hole current components compensate each other at the base-collector junction.

$$I_C = I_B = 0$$

Band diagram of a bipolar trasistor for reverse biased base-collector junction, $V_{BC} < 0$, at $V_{BE} = 0$

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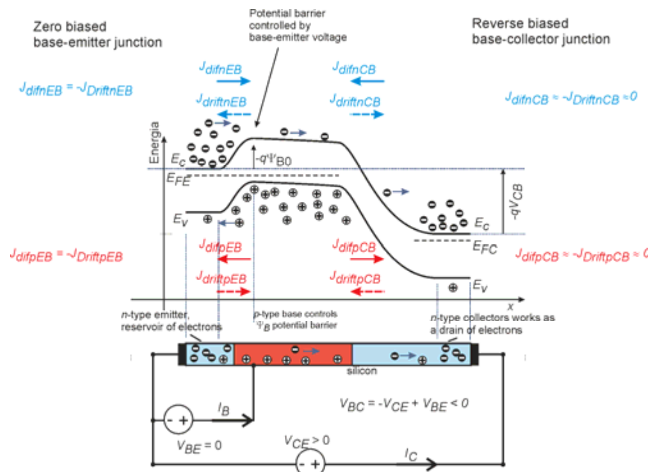
Note: arrows show directions of fluxes, not of currents.



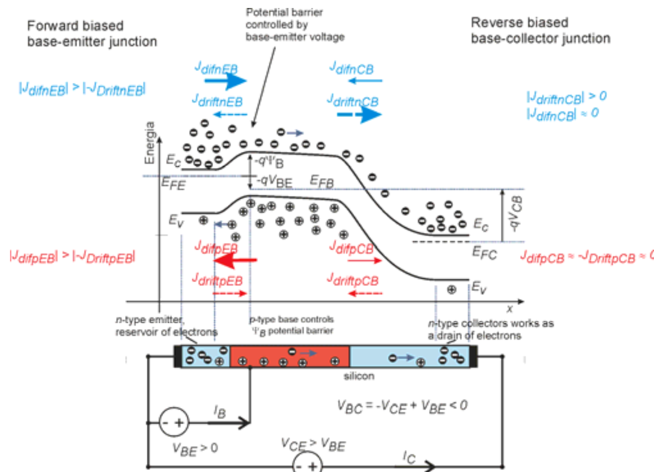
- The diffusion and drift electron current components compensate each other at the base-emitter junction. The hole currents are compensated also.
- The drift components of the electron and hole currents at the base-collector juction outbalance the diffusion components.
- Electrons from the base that arrive at the edge of the base-collector depletion layer drift towards the collector – but their concentration is small.
- Holes from the collector that arrive at the edge of the base-collector depletion layer drift towards the base – but their concentration is small.

$$I_C \approx I_B \approx 0$$

Band diagram of a bipolar trasistor for active normal bias that is at $V_{BE} > 0$ and $V_{BC} \leq 0$

158

Note: arrows show directions of fluxes, not of currents.



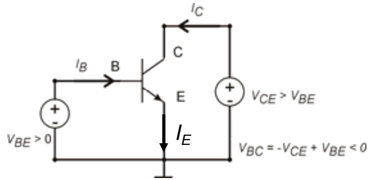
- The diffusion component of electron current is much larger than the drift component at the base-emitter junction. The same holds for holes.
- The drift components of the electron and hole currents at the base-collector juction outbalance the diffusion components.
- Electrons from the base that arrive at the edge of the base-collector depletion layer drift towards the collector – electrons are injected from emiter, their concentration is high.
- Holes from the collector that arrive at the edge of the base-collector depletion layer drift towards the base – but their concentration is small.

$I_C \geq 0$ $\quad I_B \geq 0$

usually also $I_C >> I_B$

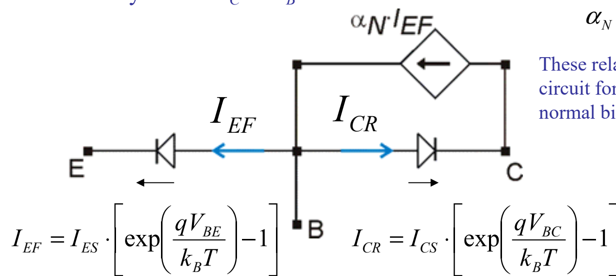
Main components of currents of *npn* transistor for active normal bias

Active normal bias of *npn* transistor



$I_C > 0$ $\quad I_B > 0$

Usually also $\quad I_C >> I_B$



$$I_{EF} = I_{ES} \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T}\right) - 1\right] \qquad I_{CR} = I_{CS} \cdot \left[\exp\left(\frac{qV_{BC}}{k_B T}\right) - 1\right]$$

Emitter currnt may be expressed as:

$$I_E = I_C + I_B$$

$$I_E \approx I_{ES} \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T}\right) - 1\right]$$

where:

$$I_{ES} = I_{nES} + I_{pES}$$

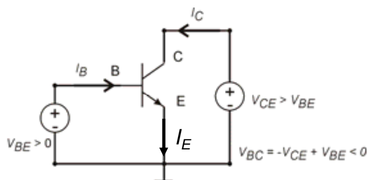
We use the index of N for current gain coefficients for active normal bias.

$$\alpha_N = \frac{I_C}{I_E} \qquad \beta_N = \frac{I_C}{I_B}$$

These relations are used for the equivalent circuit for *npn* transistor operating at the active normal bias.

DC current gain coefficients - definitions

Active normal bias of *npn* transistor



$I_C \geq 0$ $\quad I_B \geq 0$

Usually also $\quad I_C >> I_B$

DC current gain at a circuit of common emitter β:

$$\beta = \frac{I_C}{I_B}$$

DC current gain at a circuit of common base α:

$$\alpha = \frac{I_C}{I_E}$$

Looking at the circuit we note:

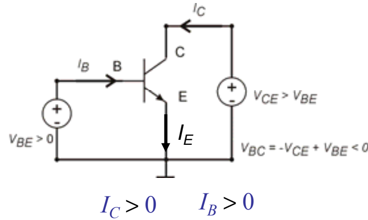
$$I_E = I_C + I_B$$

Therefore,

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{1+\beta}$$

Current gain of *npn* transistor at active normal bias

Active normal bias of *npn* transistor



$I_C > 0 \quad I_B > 0$

We know that:

$$I_C \approx I_{nE} \approx I_{nES} \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T}\right) - 1\right]$$

$$I_{nES} \approx \frac{qA_E D_{nB} n_i^2}{\int_0^{W_B} N_{AB}(x)dx}$$

$$I_B \approx I_{pE} \approx I_{pES} \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T}\right) - 1\right]$$

$$I_{pES} \approx \frac{qA_E n_i^2}{N_{DE}} \sqrt{\frac{D_{pE}}{\tau_{pE}}}$$

$$\beta_N = \frac{I_C}{I_B}$$

It can be seen that the current gain β_N is larger for the larger values of a ratio of donor concentration in emiter to acceptor concentration in a base:

$$\beta_N \propto \frac{N_{DE}}{N_{AB}}$$

The larger current gain β_N can be obtained for larger values of excess electrons and holes lifetimes, because of reduced recombination currents.

Typical values of current gain β_N are 100 – 300 for low frequency transistors, and 10 – 100 for radio frequency transistors.

Saturation operation region – both junctions, base-emitter and base-collector, forward biased.

- The base-collector junction can be also forward biased. When the both junctions are forward bias we refer to this operation mode as to operation at saturation.
- Concentrations of both, electrons and holes in the base exceed the equilibrium values.

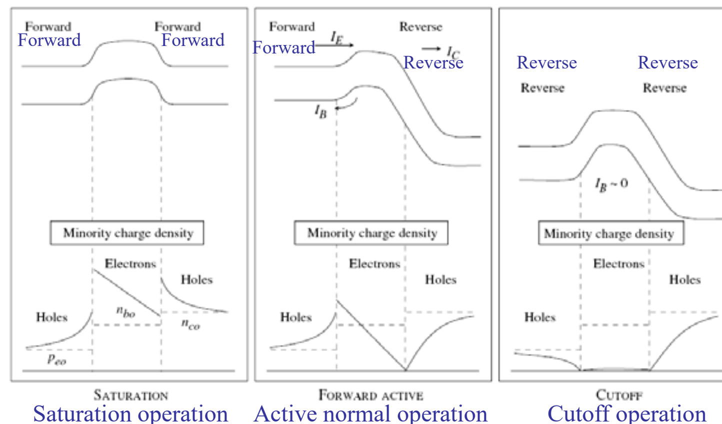
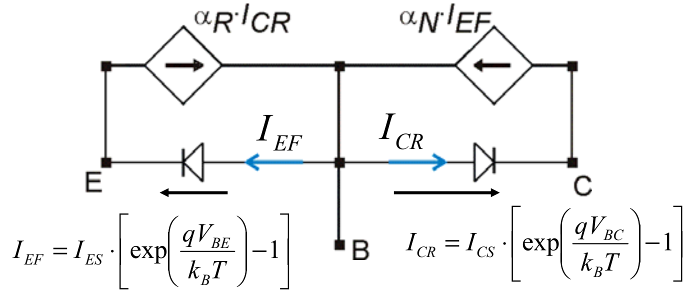


Figure 6.8: The band profile and minority charge distribution in a BJT under saturation, forward active, and cutoff modes.

From: U.Mishra, J.Singh "Semiconductor Device Physics and Design", Springer 2007

DC Ebers-Moll equivalent transistor model used for computer circuit simulation and design



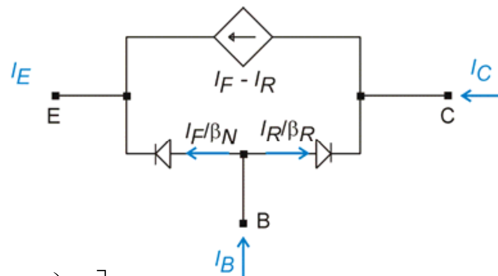
$$I_{EF} = I_{ES} \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T} \right) - 1 \right] \qquad I_{CR} = I_{CS} \cdot \left[\exp\left(\frac{qV_{BC}}{k_B T} \right) - 1 \right]$$

- Symmetry of the equivalen circuit is related to the symmetry of the *npn* transistor structure. Differences in distributions of dopants at the emiter and collector result in different values of the model parameters.
- The model applies for any combination of base-emiter and base-collector bias – forward or reverse.
- The current gain α_R for the active reverse operation ($V_{BE} < 0$, $V_{BC} > 0$) is usually smaller than the α_N value for active normal operation.

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$

- The current gain β_R for the active reverse operation ($V_{BE} < 0$, $V_{BC} > 0$) is usually small, in the range of 1-10. It is a result of a lower dopant concentration at a collector than at an emitter.

DC transport model used for SPICE program



$$I_F = I_S \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T} \right) - 1 \right] \qquad I_R = I_S \cdot \left[\exp\left(\frac{qV_{BC}}{k_B T} \right) - 1 \right]$$

$$\beta_N \equiv \beta$$

$$I_S = \alpha_N \cdot I_{ES} = \alpha_R \cdot I_{CS}$$

There are only 3 DC parameters of the model:
I_S , β_N , β_R

DC transport model used for SPICE program simplified for active normal operation

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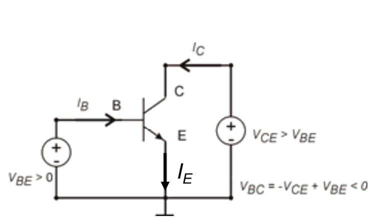

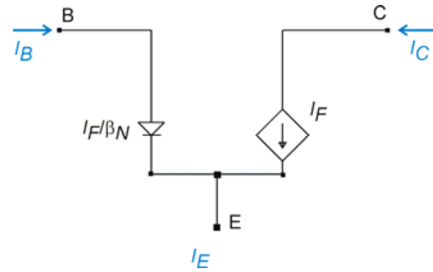

$$I_F = I_S \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T} \right) - 1 \right]$$

$$\beta_N \equiv \beta$$

DC parameters of the model :
I_S , β_N

Static characteristics of ideal bipolar npn transistor

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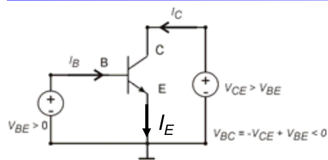
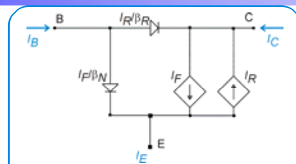
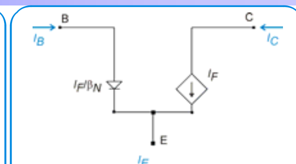




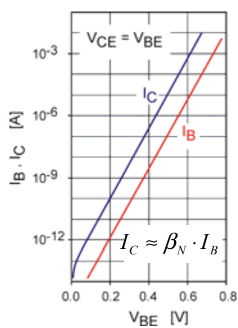
$$I_R = I_S \cdot \left[\exp\left(\frac{qV_{BC}}{k_B T} \right) - 1 \right]$$

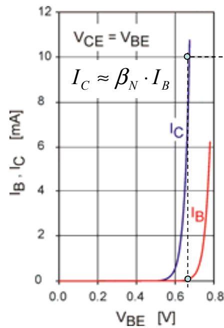
Model parameters:
I_S , β_N , β_R

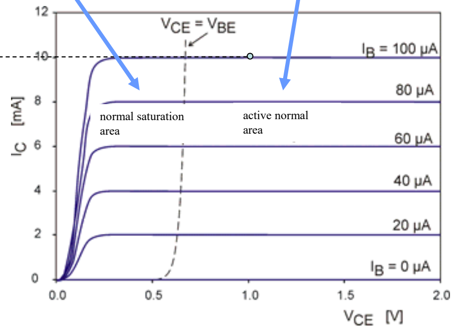


$$I_F = I_S \cdot \left[\exp\left(\frac{qV_{BE}}{k_B T} \right) - 1 \right]$$

Model parameters :
I_S , β_N







2SA1252 / 2SC3134 — PNP / NPN Epitaxial Planar Silicon Transistors

pnp npn

High VEBO, AF Amp Applications

Characteristics of real bipolar transistors

from catalog of SANYO Co.

Features

- High VEBO.
- Wide ASO and high durability against breakdown.

Specifications ( ) : 2SA1252

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		(–)60	V
Collector-to-Emitter Voltage	V_{CEO}		(–)50	V
Emitter-to-Base Voltage	V_{EBO}		(–)15	V
Collector Current	I_C		(–)150	mA
Collector Current (Pulse)	I_{CP}		(–)300	mA
Collector Dissipation	P_C		200	mW
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		–55 to +150	°C

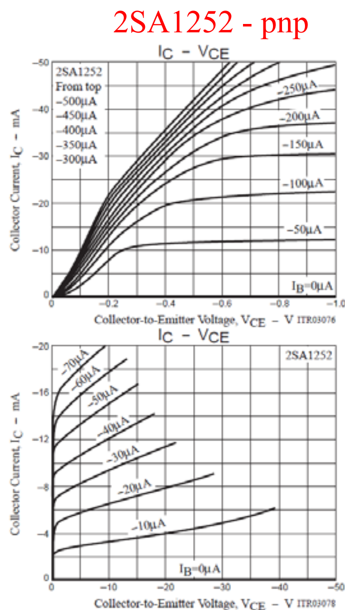
Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Collector Cutoff Current	I_{CBO}	V_{CB}=(–)40V, I_E=0A			(–)0.1	µA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(–)10V, I_C=0A			(–)0.1	µA
DC Current Gain	h_{FE}	V_{CE}=(–)6V, I_C=(–)1mA	90*		600*	
Gain-Bandwidth Product	f_T	V_{CE}=(–)6V, I_C=(–)1mA		100		MHz
Output Capacitance	Cob	V_{CB}=(–)6V, f=1MHz		(3.5)2.2		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=(–)50mA, I_B=(–)5mA			(–)0.5	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=(–)10µA, I_E=0A	(–)60			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=(–)1mA, R_{BE}=∞	(–)50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=(–)10µA, I_C=0A	(–)15			V

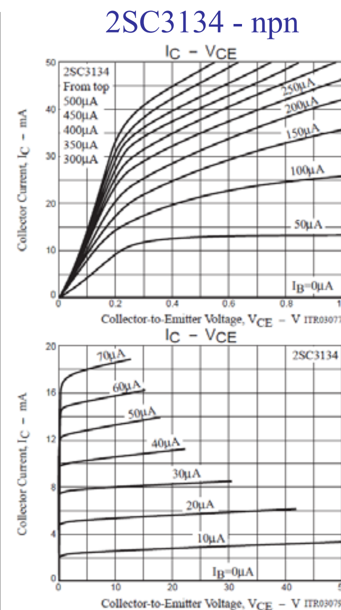
Characteristics of real bipolar transistors

from catalog of SANYO Co.

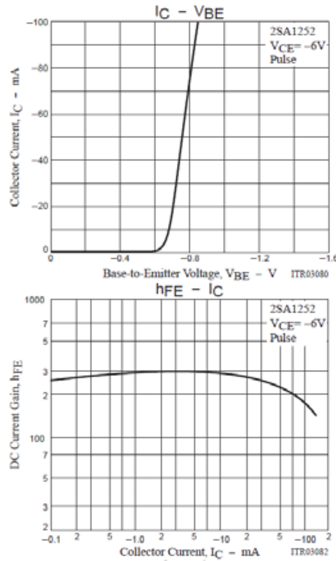
2SA1252 - pnp



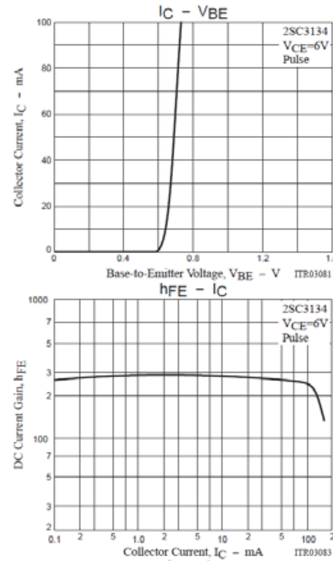
2SC3134 - npn



2SA1252 - pnp



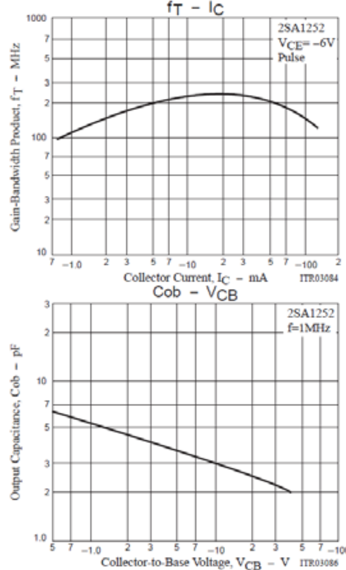
2SC3134 - npn



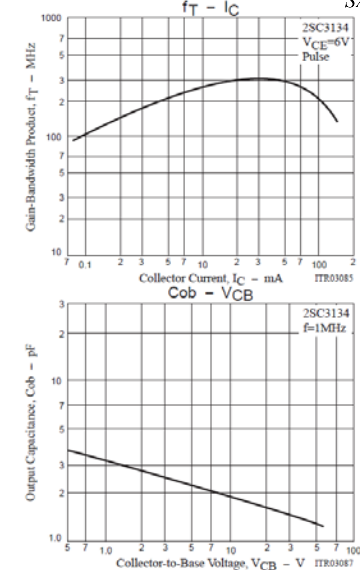
from catalog of SANYO Co.

$$h_{FE} \equiv h_{21e} \approx \beta_N$$

2SA1252 - pnp



2SC3134 - npn

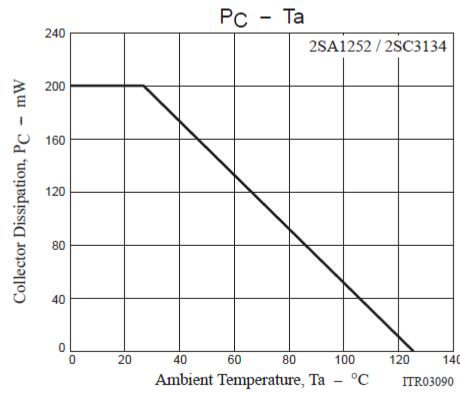


from catalog of SANYO Co.

Characteristics of real bipolar transistors

2SA1252 - pnp | 2SC3134 - npn

from catalog of SANYO Co.

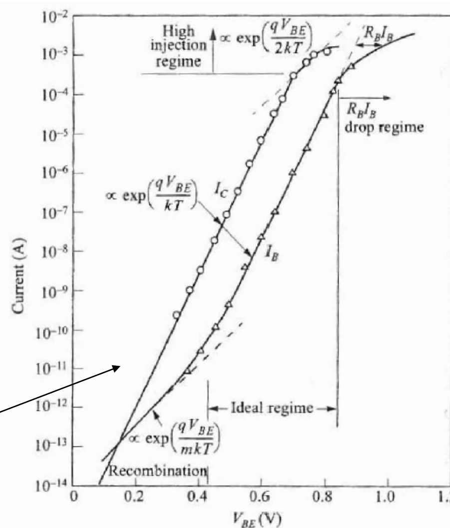


Dopuszczalna moc wydzielana w tranzystorach w funkcji temperatury otoczenia.

Output and transfer characteristics of *npn* transistor at active normal bias

The characteristics are measured at $V_{BC} = 0$, which is at $V_{BE} = V_{CE}$. They enable estimation of saturation current values and current gain values used for computer models of transistors.

Characteristics of a real transistor



Collector and base currents as a function of base-emitter voltage. (A

S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006

Output characteristics of *npn* transistor working at common emiter configuration

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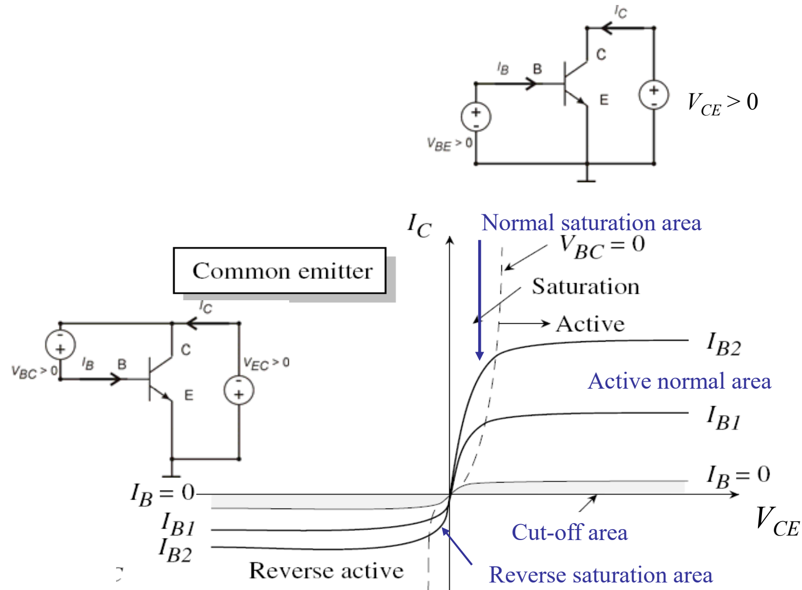
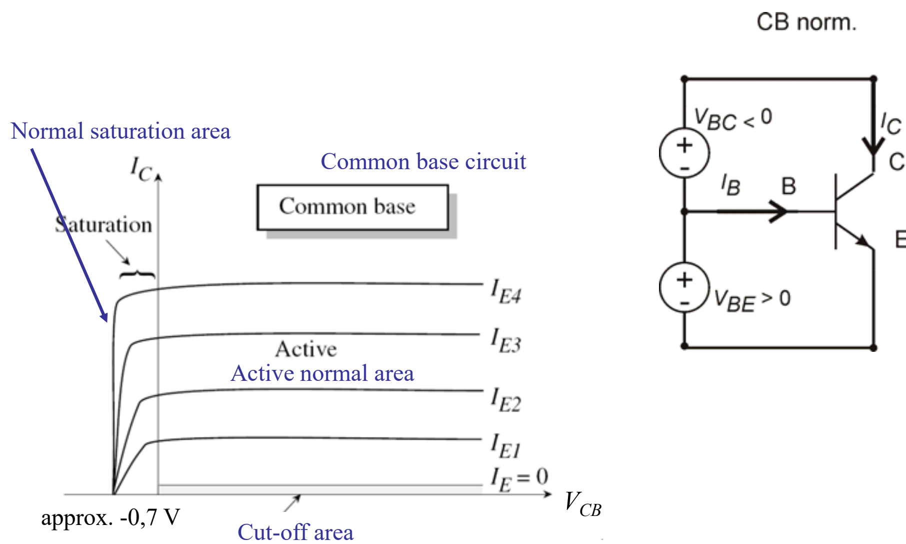


from: U.Mishra, J.Singh "Semiconductor Device Physics and Design", Springer 2007

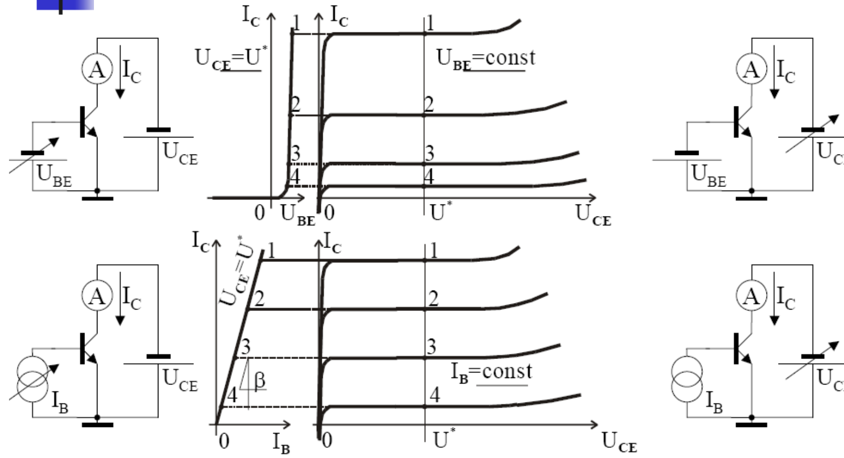
Output characteristics of *npn* transistor working at common base configuration

174



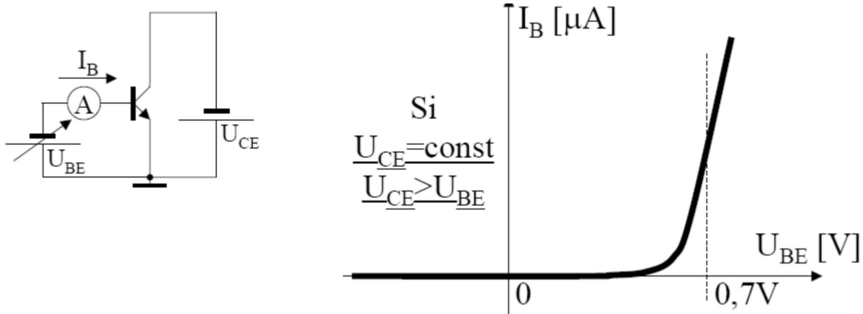
rys: U.Mishra, J.Singh "Semiconductor Device Physics and Design", Springer 2007

Output and transfer characteristics of *npn* transistor



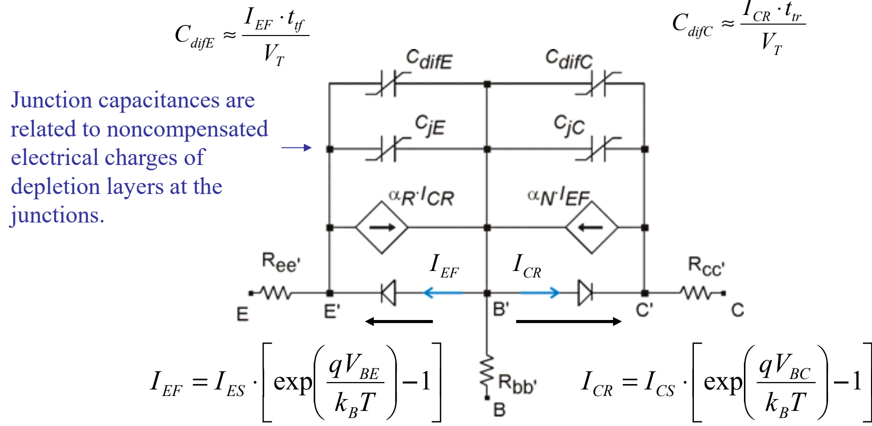
Author: Prof. dr hab. inż. M. Polowczyk

Input characteristic of *npn* transistor



Author: Prof. dr hab. inż. M. Polowczyk

Diffusion capacitances are related to injection of excess minority electrons and holes in the junctions.



Here t_{tf}, t_{tr} – are transit times of electrons and holes (equal in ideal case).

S.M.Sze, Kwok K.Ng, Physics of Semiconductor Devices, 3 ed, Wiley, 2006

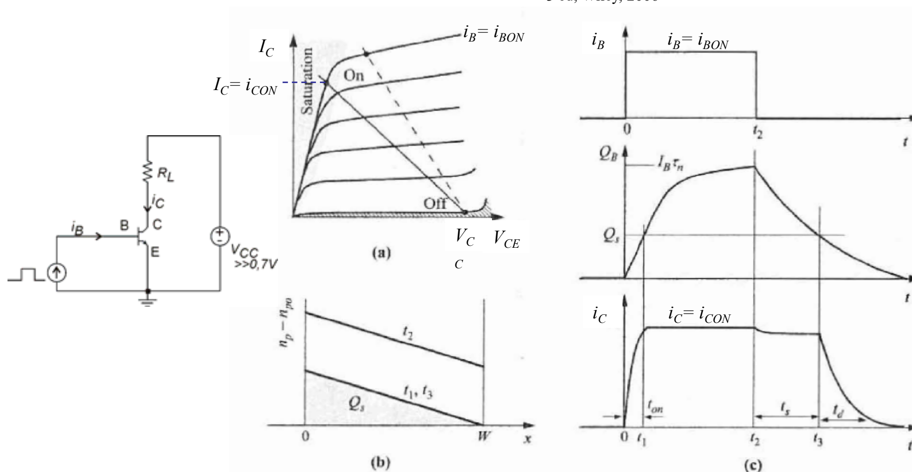
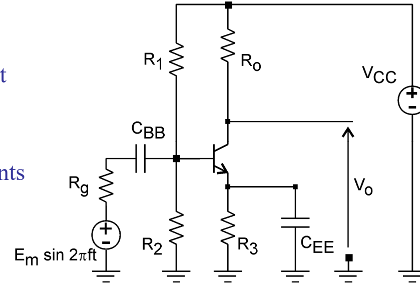


Fig. 20 (a) On-state and off-state operating points in a common-emitter configuration. Dashed line indicates restricting the on-state in the normal mode to avoid storage time t_s. (b) Minority-carrier profile in the base at different time. (c) Response of Q_B and J_C to a step base-current input.

Linearization of transistor model for a DC operation point belonging to active normal area

Let us bias a transistor so that its DC operation point belong to the active normal area $V_{BEdc} > 0$, $V_{CEdc} > V_{BEdc}$. For this purpose we use $R_1 - R_3$, R_0 and V_{cc} at our circuit.

Let the magnitude E_m of the AC voltage source be small, so that the variations of the voltages and currents $v_{be}(t)$, $v_{ce}(t)$, $i_b(t)$, $i_c(t)$ are very small as compared to their DC components V_{BEdc}, V_{CEdc}, I_{Bdc}, I_{Cdc}.



At these conditions, the I-Vs (the relations between the currents and voltages of the transistor) can be approximated with straight lines tangential to the I-Vs at the DC operating piont:

$$i_c(t) \approx I_{Cdc} + \left.\frac{dI_C}{dV_{be}}\right|_{I_C=I_{Cdc}} \cdot [v_{be}(t) - V_{BEdc}] \approx I_{Cdc} + \left.g_m\right|_{I_C=I_{Cdc}} \cdot V_{be} \cdot \sin(2\pi f)$$

Transconductance of the transistor:

$$g_m = \left.\frac{dI_C}{dV_{be}}\right|_{I_C=I_{Cdc}} \approx \frac{I_{Cdc}}{n_{ideal}V_T} \approx \frac{I_{Cdc}}{V_T}$$

$$i_b(t) \approx I_{Bdc} + \left.\frac{dI_B}{dV_{be}}\right|_{I_C=I_{Cdc}} \cdot [v_{be}(t) - V_{BEdc}] \approx I_{Bdc} + \left.g_{be}\right|_{I_C=I_{Cdc}} \cdot V_{be} \cdot \sin(2\pi f)$$

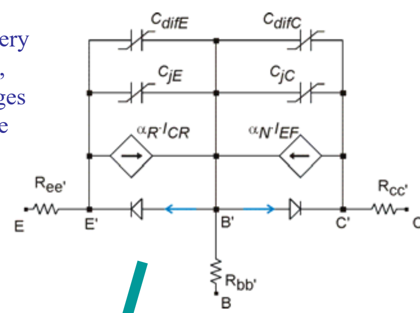
Base-emitter differential conductivity:

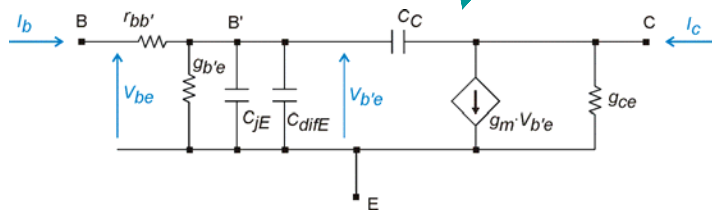
$$g_{be} = \left.\frac{dI_B}{dV_{be}}\right|_{I_C=I_{Cdc}} \approx \frac{I_{Bdc}}{n_{ideal}V_T} \approx \frac{I_{Bdc}}{V_T}$$

Linearization of transistor model for a DC operation point belonging to active normal area

Under the condition that the time variations of the voltages and currents $v_{be}(t)$, $v_{ce}(t)$, $i_b(t)$, $i_c(t)$ are very small as compared to their DC components V_{BEdc}, V_{CEdc}, I_{Bdc}, I_{Cdc}, the AC components of the voltages and currents can be calculated with the help of the linearized transistor model -

1) we calculate or measure the DC bias point of the transistor - V_{BEdc}, V_{CEdc}, I_{Bdc}, I_{Cdc};
2) and use these values for estimation of the parameters of the linearized transistor model.



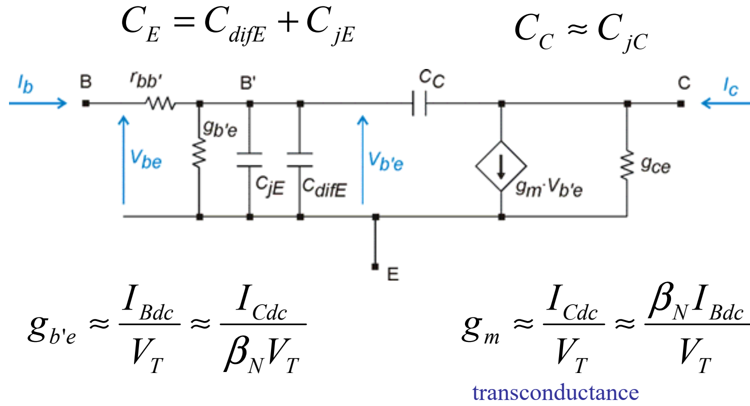


Small signal transistor model
for a DC operation point belonging to active normal area

1) It is known the DC bias point of the transistor - V_{BEdc}, V_{CEdc}, I_{Bdc}, I_{Cdc};
2) these values are used for estimation of the parameters of the linearized transistor model.

The capacitances are approximated as fixed values, but depending on DC components of currents and voltages of the transistor - V_{BEdc}, V_{CEdc}, I_{Bdc}, I_{Cdc}

$$C_E = C_{difE} + C_{jE} \qquad C_C \approx C_{jC}$$

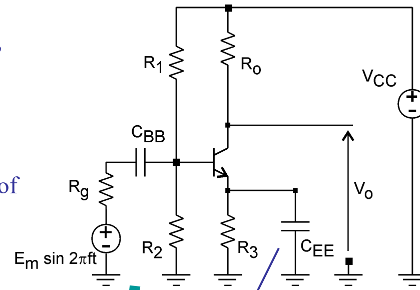


$$g_{b'e} \approx \frac{I_{Bdc}}{V_T} \approx \frac{I_{Cdc}}{\beta_N V_T} \qquad g_m \approx \frac{I_{Cdc}}{V_T} \approx \frac{\beta_N I_{Bdc}}{V_T}$$

transconductance

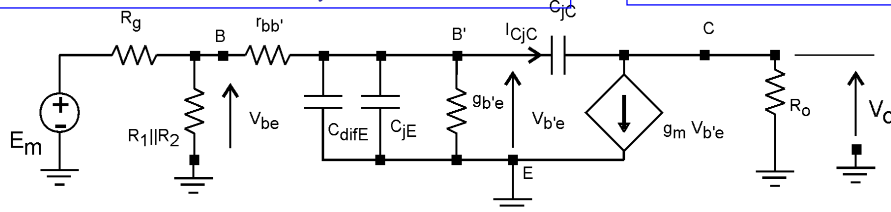
Small signal circuit model
for a DC operation point belonging to active normal area

1) DC bias point of the transistor, V_{BEdc}, V_{CEdc}, I_{Bdc}, I_{Cdc} - already known;
2) these values were used for estimation of the parameters of the linearized transistor model;
3) we use the principle of superposition to obtain a small signal circuit model, useful for calculation of AC components of voltages and currents.



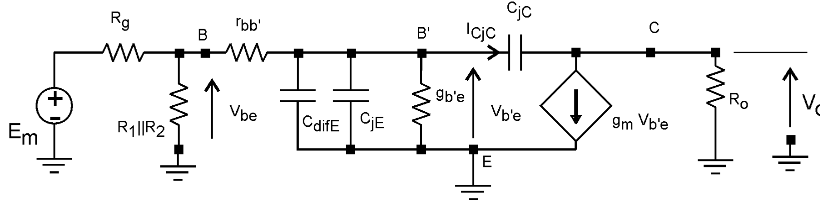
C_{EE} and C_{BB} were assumed to be very large - they may be considered as short circuits for AC analysis.

Independent DC voltage sources are modeled as short circuits, and independent DC current sources are modeled as open circuits for AC analysis.
C_{EE} and C_{BB} were assumed to be very large, so that they may be considered as short circuits for AC analysis.



Small signal circuit model for a DC operation point belonging to active normal area

1) DC bias point of the transistor, V_{BEdc}, V_{CEdc}, I_{Bdc}, I_{Cdc} - already known;
2) these values were used for estimation of the parameters of the linearized transistor model;
3) we obtain a small signal circuit model, useful for calculation of AC components of voltages and currents;



4) the AC components of voltages and currents are calculated then;
5) the AC components and DC components are added to obtain the momentary values of voltages and currents.

$$i_c(t) \approx I_{Cdc} + I_c \cdot \sin(2\pi ft) \qquad i_b(t) \approx I_{Bdc} + I_b \cdot \sin(2\pi ft)$$

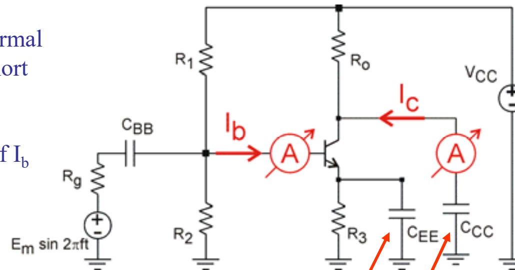
$$v_{ce}(t) \approx V_{CEdc} + V_{ce} \cdot \sin(2\pi ft) \qquad v_{be}(t) \approx V_{BEdc} + V_{be} \cdot \sin(2\pi ft)$$

Note: V_{be}, V_{ce}, I_b, I_c – *complex amplitudes of AC components.*

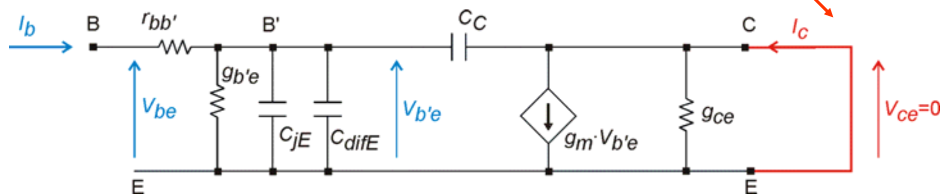
Forward short-circuit current gain h_{21e}

Let us bias a transistor so that its DC operation point belong to the active normal area $V_{BEdc} > 0$, $V_{CEdc} > V_{BEdc}$. Let us short the collector with the emiter using a capacitance of very large value. Let us measure the AC complex amplitudes of I_b and I_c.

$$h_{21e} = \left. \frac{I_c}{I_b} \right|_{V_{ce}=0}$$

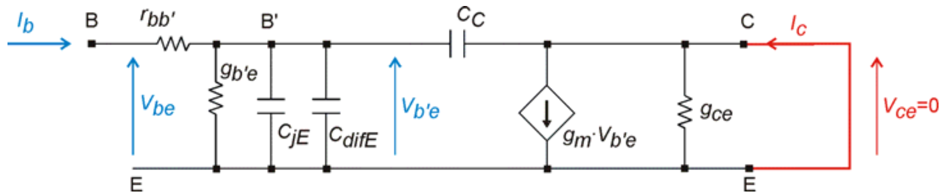


Short-circuit for alternating current



Small signal equivalent circuit of the transistor and the shorting capacitor.

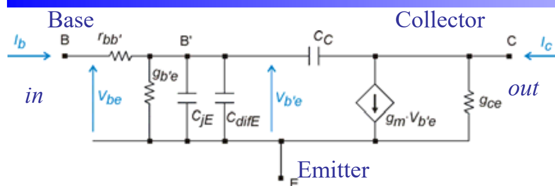
Forward short-circuit current gain h_{21e}



$$h_{21e} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0} \qquad h_{21e} = \frac{g_m}{g_{be} + j\omega \cdot (C_{jE} + C_{difE})} \qquad \frac{g_m}{g_{be}} = \beta_N$$

$$\frac{C_{difE} + C_{jE} + C_{jC}}{g_{be}} = \frac{1}{\omega_\beta} = \frac{1}{2\pi \cdot f_\beta} \qquad h_{21e} = \frac{\beta_N}{1 + j\dfrac{f}{f_\beta}}$$

Two-port network models of transistor (for common emitter configuration)



Small signal equivalent transistor circuit is a two-port network.
Emitter is common for the input port – base, and for the output port – collector;
- a common emitter circuit.

$i_b = i_1$, $v_{be} = v_1$
$i_c = i_2$, $v_{ce} = v_2$

$$V_{be} = h_{11e} I_b + h_{12e} V_{ce}$$
$$I_c = h_{21e} I_b + h_{22e} V_{ce}$$

hybrid equations

$$I_b = y_{11e} V_{be} + y_{12e} V_{ce}$$
$$I_c = y_{21e} V_{be} + y_{22e} V_{ce}$$

admitance equations

$$V_{be} = z_{11e} I_b + z_{12e} I_c$$
$$V_{ce} = z_{21e} I_b + z_{22e} I_c$$

impedance equations

Current gain:

$$h_{21e}(f) = \left.\frac{I_c(f)}{I_b(f)}\right|_{Vce=0}$$

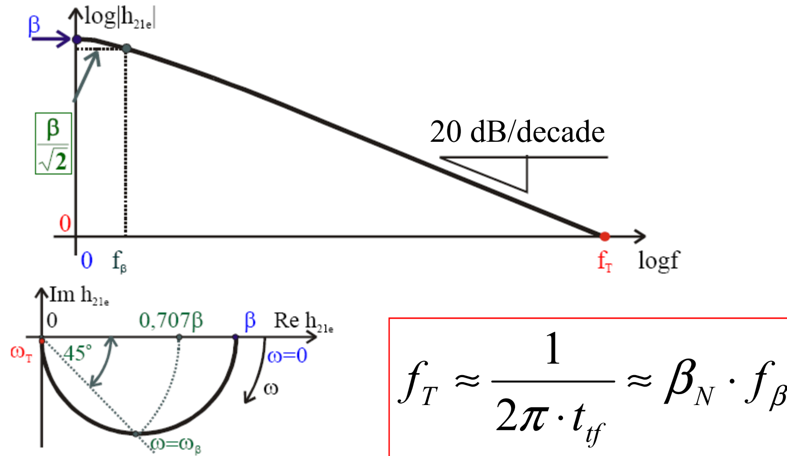
For bipolar transistors:

$$f \to 0$$
$$\Rightarrow h_{21e}(f) \to \beta_N$$

Transistor transconductance:

$$g_m = y_{21e} = \left.\frac{I_c}{V_{b'e}}\right|_{V_{ce}=0}$$

Matrices $[h_{ij}]$, $[y_{ij}]$ i $[z_{ij}]$ are equivalent and they can be transformed to calculate parameters of any type having a one type matrix. Microwave engineers use $[S_{ij}]$ - other equivalent matrix.



$$f_T \approx \frac{1}{2\pi \cdot t_{tf}} \approx \beta_N \cdot f_\beta$$

t_{tf} - transit time of electrical charge carriers for active normal bias

Author: Prof. dr hab. inż. M. Polowczyk

The cut-off frequency of current gain f_T is defined as the frequency at which the common-emitter short-circuit current gain drops to the value of 1.

$$f_T \approx \frac{g_m}{2\pi\left(C_{difE} + C_{jE} + C_{jC}\right)} \qquad g_m \approx \frac{I_{Cdc}}{V_T} \approx \frac{\beta_N I_{Bdc}}{V_T}$$

We can measure the cut-off frequency of current gain f_T at a large value of I_C , so that the junction capacitances related to the depletion layers are neglible in comparison to the diffusion capacitance C_{difE} . The C_{difE} value may be used for calculation of the transit time t_{tf} and for obtaining its dependence on $I_C \approx I_{EF}$

$$C_{difE} \approx \frac{I_C \cdot t_{tf}}{V_T}$$

The cut-off frequency of power gain f_{max} is defined as the frequency at which the extrapolated common-emitter power gain drops to the value of 1.

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi \cdot r_{bb'} C_{jC}}}$$

Determination of cut-off frequencies

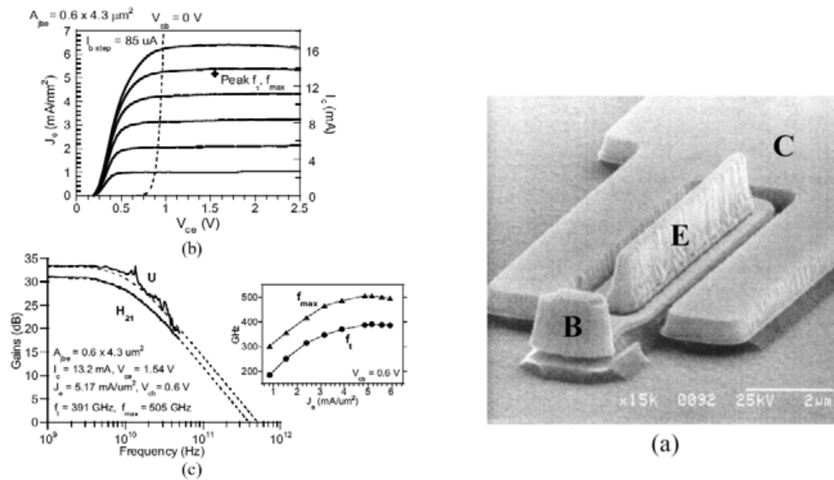
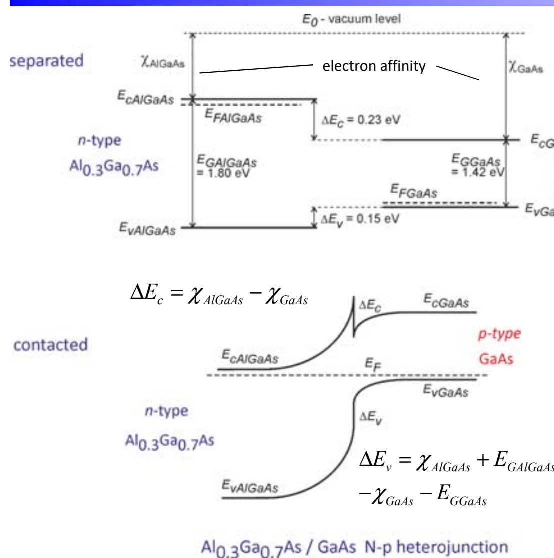


Figure 6.1: State of the art n-InP/p^+-InGaAs/n^--InP double heterojunction bipolar transistor (DHBT). (a)SEM image of device, (b) dc I-V characteristics, and (c) high frequency current gain and power gain. For this device, the average $\beta \approx 36$ and $V_{BR,CEO} = 5.1$ V (measured at $I_C = 50\ \mu A$). Figures courtesy of M. Rodwell and Z. Griffith, UCSB.

rys: U.Mishra, J.Singh "Semiconductor Device Physics and Design", Springer 2007

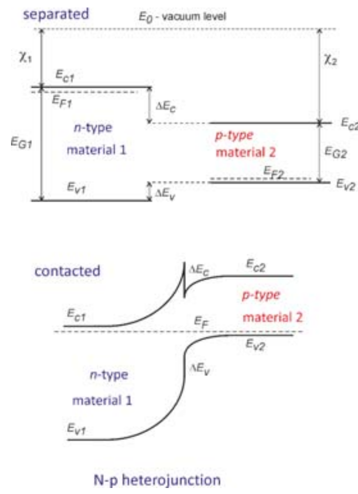
Semiconductor heterojunction



- Heterojunction – junction of different semiconductors, e.g. $Al_xGa_{1-x}As$ and GaAs, usually of different bandgaps E_G .
- Important application – for heterojunction transistors.
- Another application - in optoelectronic devices to obtain direct bandgap or to tune wavelengths of emitted or absorbed light or to minimize the volume of crystal where radiative recombination of electrons and holes takes place.
- In thermal equilibrium, after bringing the materials into contact, the Fermi energy levels E_F align.
- But, the differences in workfunctions of the materials make the band offsets ΔE_c and ΔE_v not changed.
- Aligning of E_F indicate existence of built-in potential difference V_{bi} between the materials:

$$-qV_{bi} = [\chi_{GaAs} + (E_{cGaAs} - E_{FGaAs})] - [\chi_{AlGaAs} + (E_{cAlGaAs} - E_{FAlGaAs})]$$

Semiconductor heterojunction



Electron concentration: $$n \approx N_C^* \exp\left(-\frac{E_c - E_{Fn}}{k_B T}\right)$$

$$E_c - E_{Fn} \approx -k_B T \ln\left(\frac{n}{N_C^*}\right) = k_B T \ln\left(N_C^*\right) - k_B T \ln(n)$$

Material workfunction: $$W \approx \chi - k_B T \ln\left(\frac{n}{N_C^*}\right)$$

Built-in potential V_{bi}:

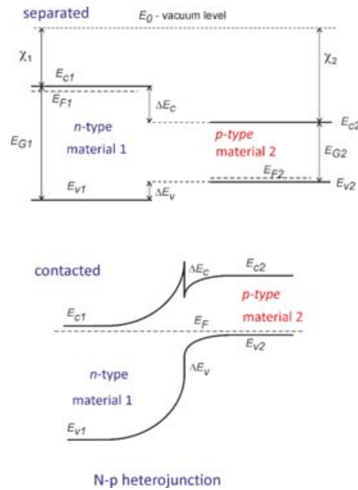
$$-qV_{bi} = \chi_2 + (E_{c2} - E_{F2}) - \chi_1 + (E_{c1} - E_{F1})$$

Its derivative V_{bi}:

$$-q\frac{dV_{bi}}{dx} = \frac{d\chi}{dx} + \frac{d}{dx}(E_c - E_F)$$

$$-q\frac{dV_{bi}}{dx} = \frac{d\chi}{dx} + k_B T\frac{dN_C^*}{N_C^*\,dx} - k_B T\frac{dn}{n\,dx}$$

Semiconductor heterostructure



We need to derive an expression for J_n suitable for heterostructure systems. Let us include an additional component A, which we do not know now, in the expression for a homostructure material:

$$J_n = qn\mu_n\mathscr{E} + qD_n\frac{dn}{dx} + A$$

Suppose that our sample is at thermal equilibrium:

$$0 = qn\mu_n\mathscr{E} + qD_n\frac{dn}{dx} + A$$

where:

$$\mathscr{E} = -\frac{dV_{bi}}{dx} \quad \text{and:} \quad \frac{dV_{bi}}{dx} = -\frac{1}{q}\frac{d\chi}{dx} - V_T\frac{dN_C^*}{N_C^*\,dx} + V_T\frac{dn}{n\,dx}$$

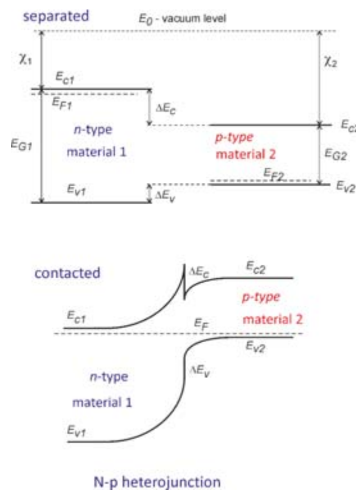
$$A = qn\mu_n\left(-\frac{1}{q}\frac{d\chi}{dx} - V_T\frac{dN_C^*}{N_C^*\,dx} + V_T\frac{dn}{n\,dx}\right) - q\mu_n V_T\frac{dn}{dx}$$

$$A = qn\mu_n\left(-\frac{1}{q}\frac{d\chi}{dx} - V_T\frac{dN_C^*}{N_C^*\,dx}\right)$$

After substituting it into the expression for J_n we obtain:

$$J_n = qn\mu_n\left(\mathscr{E} - \frac{1}{q}\frac{d\chi}{dx} - V_T\frac{dN_C^*}{N_C^*\,dx}\right) + qD_n\frac{dn}{dx}$$

Semiconductor heterostructure



$$J_n = q n \mu_n \left(\mathscr{E} - \frac{1}{q}\frac{d\chi}{dx} - V_T \frac{dN_C^*}{N_C^* dx} \right) + q D_n \frac{dn}{dx}$$

The expression for J_n is valid not only for thermal equilibrium.

The second and third components may be interpreted as additional electric field related to varying electron affinity χ and to varying effective electron state density N_C^* , because of the bandgap engineering of the heterostructure :

$$\mathscr{E}_{hetn} = -\frac{1}{q}\frac{d\chi}{dx} - V_T \frac{dN_C^*}{N_C^* dx}$$

$$J_n = q n \mu_n \left(\mathscr{E} + \mathscr{E}_{hetn} \right) + q D_n \frac{dn}{dx}$$

The expression for J_p can be obtained similarly:

$$J_p = q p \mu_p \left(\mathscr{E} - \frac{1}{q}\frac{d\chi}{dx} - \frac{1}{q}\frac{dE_G}{dx} + V_T \frac{dN_V^*}{N_V^* dx} \right) - q D_p \frac{dp}{dx}$$

$$\mathscr{E}_{hetp} = -\frac{1}{q}\frac{d\chi}{dx} - \frac{1}{q}\frac{dE_G}{dx} + V_T \frac{dN_V^*}{N_V^* dx}$$

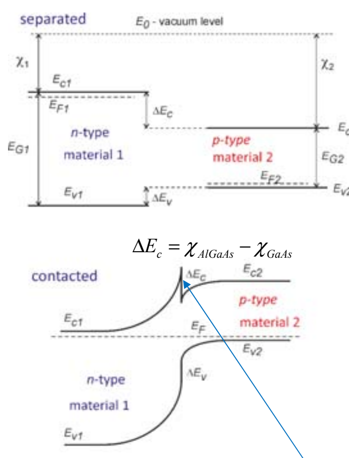
$$J_p = q p \mu_p \left(\mathscr{E} + \mathscr{E}_{hetp} \right) - q D_p \frac{dp}{dx}$$

Basic equations for analysis of heterostructure device operation

Poisson equation – for potential distribution V :

$$-\frac{\partial \mathscr{E}}{\partial x} = \frac{\partial^2 V}{\partial x^2} = \frac{q\left(n - p + N_A^- - N_D^+\right)}{\varepsilon\varepsilon_0}$$

Note – approximation of completely depleted layer often can be used for junction analysis.



$$\Delta E_c = \chi_{AlGaAs} - \chi_{GaAs}$$

$$\Delta E_v = \chi_{AlGaAs} + E_{GAlGaAs} - \chi_{GaAs} - E_{GGaAs}$$

Continuity equation for electrons:

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\frac{\partial \boldsymbol{J}_n}{\partial x}$$

Continuity equation for holes:

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\frac{\partial \boldsymbol{J}_p}{\partial x}$$

Density of electron conduction current:

$$J_n = q n \mu_n \left(\mathscr{E} - \frac{1}{q}\frac{d\chi}{dx} - V_T \frac{dN_C^*}{N_C^* dx} \right) + q D_n \frac{dn}{dx}$$

Density of hole conduction current:

$$J_p = q p \mu_p \left(\mathscr{E} - \frac{1}{q}\frac{d\chi}{dx} - \frac{1}{q}\frac{dE_G}{dx} + V_T \frac{dN_V^*}{N_V^* dx} \right) - q D_p \frac{dp}{dx}$$

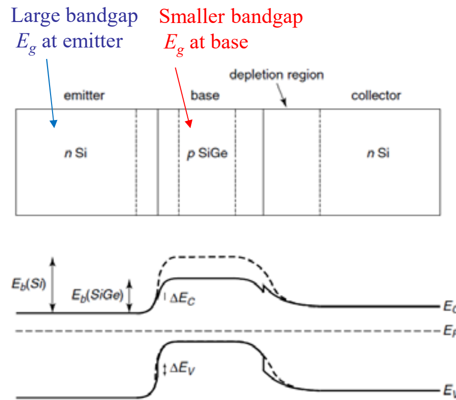
Density of total conduction current :

$$J_x = J_{nx} + J_{px}$$

Note – Quantization of electron energy levels and two-dimensional electrical charge carrier distributions should be considered for narrow potential wells of widths comparable to the carrier de Broglie wavelengths.

Heterojunction bipolar transistor

Npn transistor

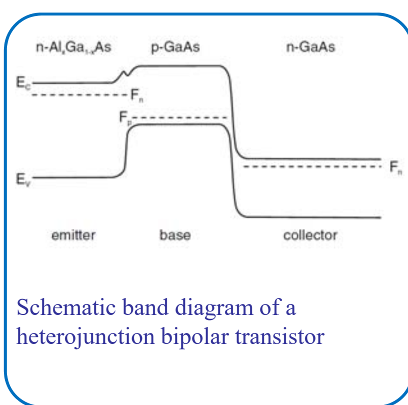


- Emitter-base heterojunction – *n*-type semiconductor of large bandgap E_G is used for emitter, and *p*-type semiconductor of small bandgap E_G is used for base.
- Semiconductors are selected so that $\Delta E_v > \Delta E_c$. Therefore, the potential barrier is larger for holes than for electrons.
- As a result, at forward E-B bias, injection of holes from base to emitter is suppressed as compared to injection of electrons from emitter to base.
- The transistor has larger current gain $\beta_N = h_{21e}$ than a homojunction transistor.
- Or, the base acceptor concentration may be increased. The value of $\beta_N = h_{21e}$ is moderate, but the base series resistance $r_{bb'}$ is reduced. This way the cut-off frequency of power gain f_{max} is inreased:

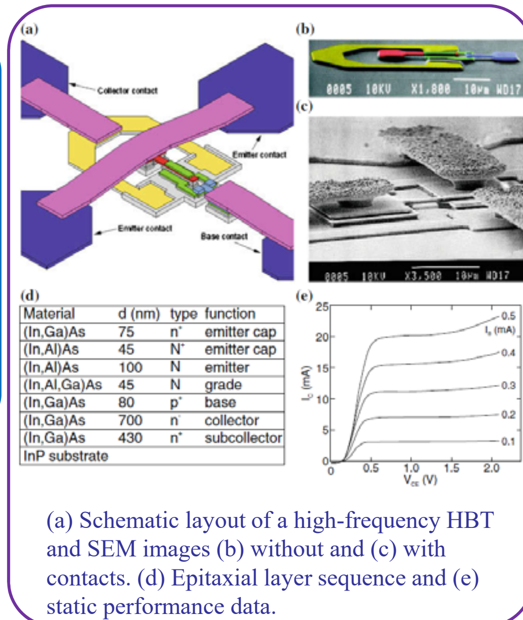
$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi \cdot r_{bb'} C_{jC}}}$$

from:P. Ashburn, SiGe Heterojunction Bipolar Transistors, Wiley 2003

IIIV - heterojunction bipolar transistor



Schematic band diagram of a heterojunction bipolar transistor



Material	d (nm)	type	function
(In,Ga)As	75	n^+	emitter cap
(In,Al)As	45	N^+	emitter cap
(In,Al)As	100	N	emitter
(In,Al,Ga)As	45	N	grade
(In,Ga)As	80	p^+	base
(In,Ga)As	700	n^-	collector
(In,Ga)As	430	n^+	subcollector
InP substrate			

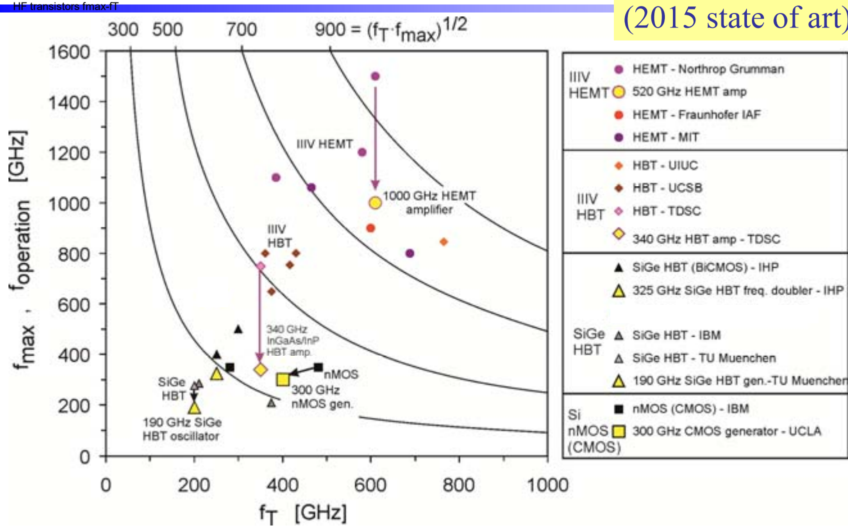
(a) Schematic layout of a high-frequency HBT and SEM images (b) without and (c) with contacts. (d) Epitaxial layer sequence and (e) static performance data.

from: M. Grundmann, The Physics of Semiconductors ..., Springer 2016

Transistors with record high f_T i f_{max} and operation frequencies of circuit $f_{circuit}$

HF transistors fmax-fT

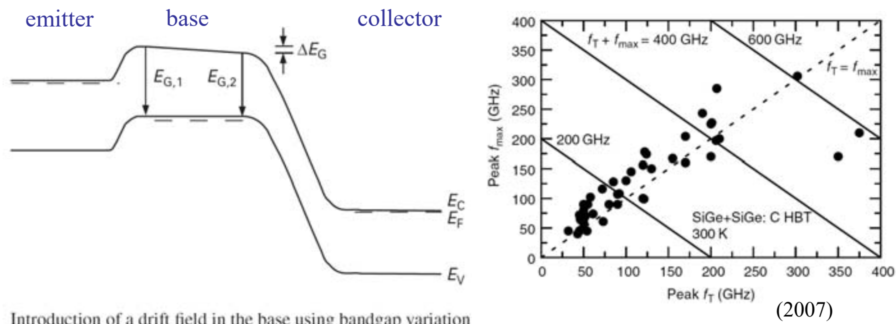
(2015 state of art)



f_{max} – cut-off frequency of power gain, at this frequency $P_{out} / P_{in} > 1$ for AC componets.

f_T – cut-off frequency of current gain, at this frequency $I_{out} / I_{in} > 1$ for AC componets.

Graded bandgap E_g at bases of N-Si/p-SiGe/N-Si heterojunction bipolar transistors



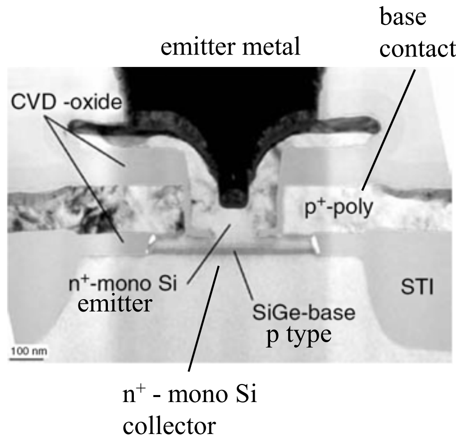
Introduction of a drift field in the base using bandgap variation

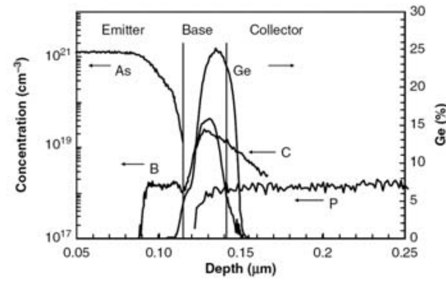
(2007)

- Larger E_g at emitter than at base is used for limitation of hole injection from the base to the emitter.
- This enables using higher concentration of acceptors at the base. I effect a series resistance of the base is reduced and, in turn, the cut-off frequency of power gain f_{max} is increased.
- Graded bandgap E_g at a base of a heterojunction bipolar transistor N-Si/p-SiGe/N-Si acts as an additional built-in electric field, which accelerates electron motion through the base. The E_g badgap grading is obtained with graded Ge content - 30% - 0% typically.

rys: J. D. Cressler, "SiGe and Si Strained-Layer Epitaxy for Silicon Heterostructure Devices", CRC 2007

N-Si/p-SiGe/N-Si heterojunction bipolar transistors fabricated with BiCMOS technology



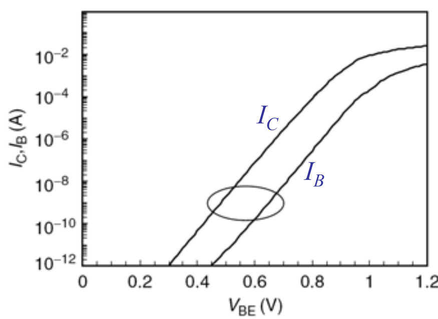


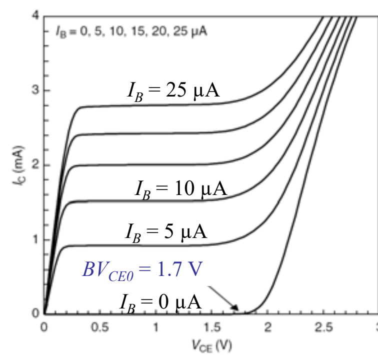
TEM cross section of a transistor with effective emitter width of 0.14 μm.

SIMS doping profile of the fabricated transistors.

rys: J. D. Cressler, "SiGe and Si Strained-Layer Epitaxy for Silicon Heterostructure Devices", CRC 2007

N-Si/p-SiGe/N-Si heterojunction bipolar transistors fabricated with BiCMOS technology

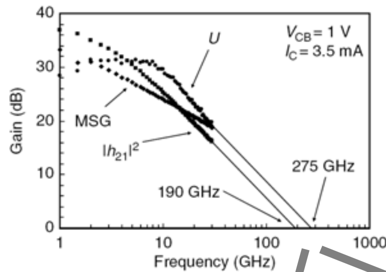




Transfer characteristics of a transistor with A_E = 0.14 x 2.6 μm^2

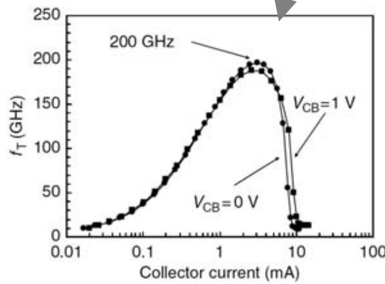
Common emitter output characteristics of a transistor with A_E = 0.14 x 2.6 μm^2

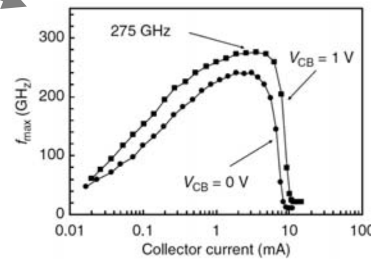
rys: J. D. Cressler, "SiGe and Si Strained-Layer Epitaxy for Silicon Heterostructure Devices", CRC 2007



Measured frequency dependence of the small signal current gain $|h_{21}|^2$, the maximum stable gain MSG, and the unilateral gain U for transistors with A_E = 0.14 x 2.6 μm²

Estimated from these type measurements values of the current gain cut-off frequency f_T and the power gain cut-off frequency f_{max}





rys: J. D. Cressler, "SiGe and Si Strained-Layer Epitaxy for Silicon Heterostructure Devices", CRC 2007

TABLE 10.1 Device Parameters of the High-Speed npn Transistor with A_E = 0.14 × 2.6 μm²

A_E	0.14 × 2.6 μm²
β	250
R_{BI}	2.8 kΩ/sq.
BV_{CE0}	1.7 V
BV_{CB0}	5.8 V
C_{EB}	6.3 fF
C_{BC}	5.5 fF
C_{CS}	3.7 fF
R_B	50 Ω
R_E	3.5 Ω
f_T	200 GHz
f_{max}	275 GHz
Gate delay(of ECL type bipolar logic gate in integrated circuit)	3.5 psec

rys: J. D. Cressler, "SiGe and Si Strained-Layer Epitaxy for Silicon Heterostructure Devices", CRC 2007

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Thank you for your attention!